Acorn Risc PC
Technical Reference Manual

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Contents

About this manual

This manual is intended as a hardware reference manual for the Acorn Risc PC .

This manual supplements the basic information given on system hardware in the *Acorn Risc PC Welcome Guide*.

The operating system is covered at the user level in the *RISC OS 3 User Guide for the Risc PC*, supplied with the computer (also available for separate purchase).

Programmers and users requiring a greater depth of information about RISC OS will also need the *RISC OS 3 Programmer's Reference Manual*, which is available from Acorn authorised dealers.

Additional detail covering the Acorn Risc PC can be found in the *RISC OS 3 Programmer's Reference Manual version 3.5 supplement* (available from Acorn authorised dealers). This is supplied with a full index covering both the *RISC OS 3 Programmer's Reference Manual* and the *RISC OS 3 Programmer's Reference Manual version 3.5 supplement*.

For datasheets covering the ARM610 and ARM700 contact:

ARM Ltd.
Fulbourn Road
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Cambridge
CB1 4JN
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Tel: 0223 400400

For datasheets covering the SMC FDC37C665, contact:

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USA

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For further information on the Risc PC range, contact:

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Histon
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CB4 4AE
UK.

Note: This manual describes various PCB assemblies. The issue of each PCB is as defined by the relevant schematic.

Important: Issue numbers

The following publications are appended to this manual:

- Acorn Guidelines for Safety Testing
- Acorn Network Card Mk II Specification
- Acorn Enhanced Expansion Card Specification

The above publications, together with the parts lists and schematics contained in this manual, are all supplied at latest issue, correct at time of printing.

Safety

These machines have been designed and certified to meet the requirements of the safety standard EN60950/BS7002. In order to meet the flammability requirements of this standard, the machines utilise flame-retardant components. As such, they should not be operated without all of the case plastics and metalwork securely fitted in place. In addition, any upgrades or modifications must not compromise these safety measures. For further advice see the *Acorn Enhanced Expansion Card Specification* (Part number 0472,200).

For checking electrical safety of the equipment after repair, or to satisfy Health and Safety regulations, see the publication on Acorn Guidelines for Safety Testing appended to this manual.

Part 1 – System description

Introduction

The Acorn Risc PC family is built around the Advanced Risc Machines (ARM) chipset, comprising the ARM processor, the I/O and Memory controller (IOMD) and the Video Controller (VIDC). All products feature IOMD and VIDC 20 and offer the following features:

- DMA Enhanced Bus Interface (DEBI) – where capabilities include 32-bit data transfer and the support of up to two general purpose DMA channels for transfer between I/O and memory
- PC-AT compatible keyboard interface
- Support for Video RAM (VRAM)
- 1-, 2-, 4-, 8-, 16- & 32-bit pixel depths
- Pixel rates in excess of 110 MHz
- Support for up to 256 MB of DRAM via two DRAM SIMM sockets
- Interchangeable ARM CPU card
- OPEN Bus connector for second bus master or additional CPU.

A block diagram of the main system components is shown in *Figure 1.1* overleaf.

General

Initially, model variants feature either an ARM 610 or ARM700 processor with the option for a Floating Point Accelerator (FPA) to plug in alongside the ARM700. The processor is resident on a small plug in card which fits in to one of the two 'OPEN Bus' slots on the main PCB. Variants are also likely to appear which feature an Intel-based processor resident in the second OPEN Bus slot.

The number of expansion bus slots available is either none, 2 or 4 (with architectural support for up to 8). The backplane PCBs are easily interchangeable as they plug into the 132-way edge connector on the main PCB. A network slot is provided so that adding network capability does not detract from the number of free expansion card slots available. This new Acorn propriety interface is, therefore, incompatible with the existing A30x0 and A4000 network expansion cards.

Memory upgrading is provided for by the use of DRAM Single In-line Memory Modules (SIMMs). Two sockets are provided for this purpose and the machine uses industry-standard modules chosen to meet the system specifications. VRAM is provided on a plug-in daughter card; this is an Acorn proprietary upgrade module and plugs into the Dual In-line Memory Module (DIMM) connector on the motherboard.

The Parallel, Serial, floppy disc and Integrated Drive Electronics (IDE) hard disc sub-systems are handled by an industry-standard PC clone Universal Peripheral Controller device (i.e. 'combo' IC). This provides PC-standard control signals and allows each of these interfaces to be (broadly) compatible with the PC world.

A new version of RISC OS 3 is provided with these machines in two 1 MB ROMS on the main PCB. This version, 3.50, provides all the necessary software and user interfaces to make use of the hardware: for instance, a new screen mode selector to cater for the increased number of screen modes available with VIDC 20. Some other functional improvements over version 3.11 have also been included. The reader is referred to the *RISC OS 3 User Guide for the Risc PC* and *RISC OS 3 Programmer's Reference Manual, Vol. 5* (version 3.5 supplement) for further details.

System chipset: ARM, IOMD, VIDC and peripheral controller

ARM

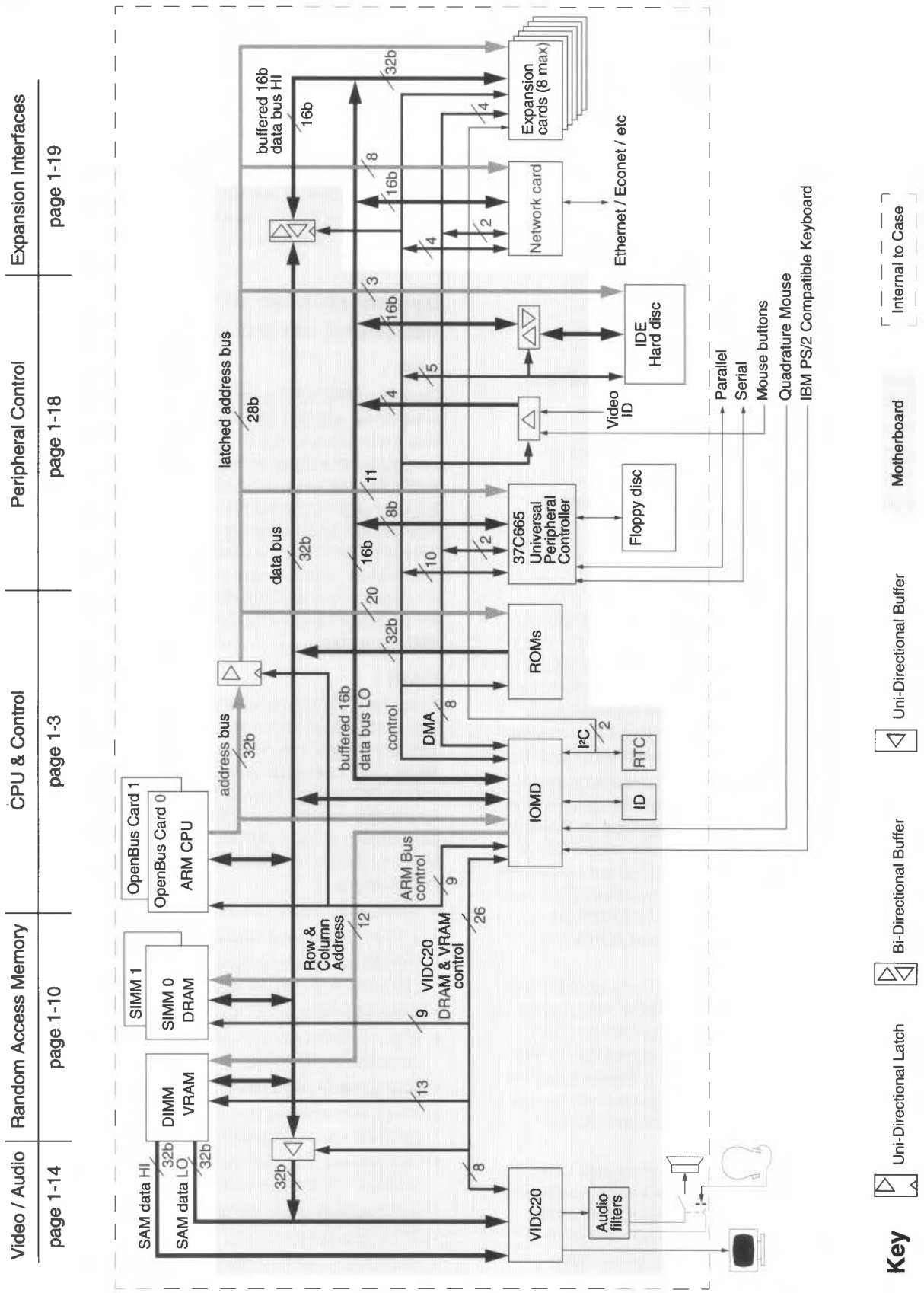
From the ARM 600 onwards, all ARM processors provide a full 32-bit address bus and a 32-bit program counter. The ARM 6x0 and 7x0 also have the ability to be configured in a 26-bit address space mode for either instruction fetches or data operations. RISC OS 3 version 3.5 operates in 26-bit address space for instruction fetches and 32-bit address space for data access. The ARM610 (and 700) also feature 4KB and 8KB caches respectively and both use write-back buffers to improve on chip memory performance. Both devices also feature an on-board memory management unit (MMU) with a 4KB page size.

IOMD

From the ARM600 onwards, the Memory Management Unit is integrated within the ARM CPU. This has allowed memory control and refresh (previously provided by MEMC), IO control (previously provided by IOC) and PC specific I/O signals to drive the PC Combo device (previously provided by IOEB) together with some new functionality to be implemented in one device: the I/O Memory Device, or IOMD. Essentially, IOMD provides the following:

- direct interface to ARM610 or ARM700
- DRAM control for 2 SIMMs providing 4 banks of DRAM
- VRAM control and interface to VIDC20, including generation of transfer cycles
- DMA Interface to CD-quality digital sound chip
- Video and sound DMA channels similar to that provided by MEMC
- four general purpose I/O DMA channels
- 16-bit byte-steered bus, for on-board peripherals such as the network and IDE interfaces
- two general purpose counter / timers and system interrupt control registers
- interrupt line allocation similar to previous machines
- PC keyboard interface
- Quadrature mouse interface.

Figure 1.1: System block diagram



VIDC

VIDC20 provides higher resolutions and colour depths than previously available on Acorn platforms. It is used in either 32 or 64-bit DRAM access mode to interface (via IOMD) with either system DRAM or 1 or 2 MB of VRAM. Although VIDC20 provides its own VRAM modes, the use of 64-bit mode allows better provision for future performance improvements. Colour depth is 1, 2, 4, 8, 16 or 32 bits per pixel and using a novel Phase Lock Loop (PLL) frequency synthesizer pixel rates are continuously selectable between 8 and 135 MHz. VIDC20 supports the old style VIDC1A 8 channel 8 bits stereo sound, but also has a high quality digital stereo 16-bit serial sound interface which is compatible with the Philips I²S standard.

Peripheral controller

The FDC37C665 Peripheral controller or 'Combo' device is memory mapped in the system IO space and connects to the lower 8 bits of the buffered data bus. This device provides the Floppy disc, Parallel and Serial interfaces, along with some of the IDE control signals, although in the system block diagram, only the IDE datapath and the IDE control signals provided by IOMD are shown.

Architecture

The block diagram in *Figure 1.1* shows how the system is built up. The ARM, second CPU, IOMD, ROMs, DRAM and VRAM (DRAM port) are all connected to the unlatched data bus. IOMD uses the unlatched processor address bus to generate the row and column addresses for the DRAM and VRAM, or suitable control signals for I/O accesses or ROM enable. The CPU data bus passes through byte steering logic internal to IOMD and emerges as the 16-bit on-board peripheral data bus BD[15:0]. This bus allows DMA data to be transferred to or from the I/O system at arbitrary byte locations. The Motherboard I/O devices use BD[15:0], which, along with the upper 16 bits of data latched by four 74ACT574s under control of IOMD, provides the 32-bit word, half word or byte wide data bus to and from the DEBI expansion interface.

CPU and control

ARM CPU & OPEN Bus

The ARM processor is fitted to a daughtercard which connects to the system via one of the OPEN Bus connectors (see *OPEN Bus* on page 2-16). The ARM 610 card contains the ARM, a 60 MHz can oscillator together with a divide by 2 circuit based on a 74ACT74 in order to ensure a clean symmetrical 30 MHz clock signal and a 74ACT08 AND gate.

System Clock generation

The master clock source, **clk64**, is a 64MHz signal which is applied to IOMD and provides all the system timing. The DRAM timing generators use both edges of a 32MHz clock, which is generated from the 64MHz by dividing by two. The peripheral bus is clocked from the master clock divided by 4 (16MHz). The video RAM serial interface uses 64MHz divided by 3 to generate **sc** which clocks the VRAM serial ports at 21.33MHz using a 2:1 mark space ratio. The VIDC20 **pclk** signal must be the same as **sc** during video RAM data transfer, but must be the same as **mclk** during cursor DMA, VIDC20 programming (**Nprog** activity), and sound DMA (if the VIDC20 sound system is being used).

In addition to **clk64** there is a 24MHz clock source which provides a reference clock to both VIDC20 and the FDC37C665 device.

IOMD

Interrupt control logic and IOC timers

IOMD has a number of interrupt inputs which can be used to generate irq and fiq interrupts. In addition, there are internal interrupts generated by the DMA channels, the keyboard interface and the IOC timers 0 and 1. A set of registers similar to those in IOC allow the interrupt sources to be controlled by the processor. Some IOC register bits are unused, and some pin polarities are different to IOC. Refer to *Figure 1.2* for the register bit allocations, and to *Table 1.1* for the interrupt active levels.

Table 1.1: Interrupt active polarities

Interrupt	Description
Npfiq	Podule fiq input. Level triggered, active low
Npirq	Podule irq input. Level triggered, active low
Nsintr	Serial interrupt input. Level triggered, active low
Nscirq	Level triggered, active low ①
Nfintr	Floppy interrupt request. Level triggered, active low
Nindex	Floppy disc index input. Falling edge triggered
flyback	Flyback from VIDC, rising edge triggered
fdrq	Floppy drq interrupt. Level triggered, active high
pintr	Printer interrupt request. Rising edge triggered

Table 1.1: Interrupt active polarities

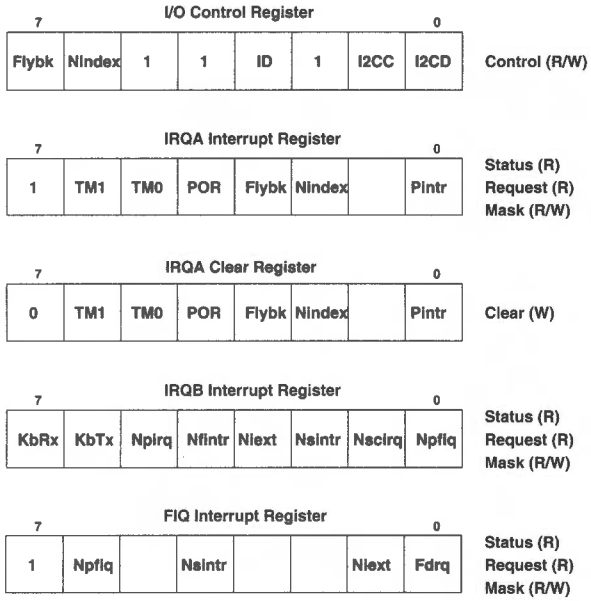
Interrupt	Description
Niext	Level triggered, active low ②

① This signal is the IDE interrupt signal inverted.

② This signal is the Network card interrupt signal inverted.

There is a control register which provides access to a small number of I/O pins. These are used for the I²C interface, and for the ID chip interface. The ID pin is held low during reset, and then tri-stated. The I²C interface pins are tri-stated on reset. The registers are also shown in *Figure 1.2*. The functionality of these registers is similar to the corresponding registers in IOC, except it is not possible to generate a FIQ from the ID I/O bit, and not all the bits in the registers are implemented. Refer to the IOC data sheet, and *Figure 1.2* for further detail.

Figure 1.2: I/O Control and Interrupt Registers



Two timers, the same as those in IOC are provided, which are clocked at the same 2MHz rate. Note that the IOC documentation is incorrect in stating that Tinterval = latch/2µS, it should say (latch+1)/2µS. Note also that if a latch command is issued immediately after a go command, the value latched may be the new value, but may be the old value of the counter. This also occurs in IOC, and should therefore not be a problem.

DMA

There are four general purpose I/O DMA channels, and two sound channels. In addition, there are two further channels for video and cursor data. The DMA channels have fixed priorities as shown below.

Table 1.2: DMA channels priority

Priority	Channel
0 (highest)	Cursor and DRAM Video
1	Sound chan. 0 (VIDC sound out and linear sound in)
2	VRAM transfer cycle
3	Sound chan. 1 (linear sound out)
4	DRAM and VRAM refresh
5	I/O DMA channels ('round robin between channels 0 to 3)
6 (lowest)	ARM

The state machine which controls bus activity has a number of points at which arbitration for the bus takes place. Arbitration always takes place while the processor performs an idle cycle and before it starts a memory access. In addition, arbitration occurs during sequential memory accesses as follows:

- DRAM/VRAM – sequential bursts of up to 8 words can occur uninterrupted by DMA. In the absence of DMA requests these bursts can extend to 256 words.
- ROM – uninterrupted burst accesses of up to 4 words can occur. If non-burst ROM is used, arbitration occurs on every access.
- PROG – uninterrupted bursts of up to 4 words can occur where the access is to an IOMD internal register. Where the access is to the VIDC control register, arbitration occurs on every word.
- I/O – an IORQ/IOGT mechanism is used for programmed I/O and (non-I/O) DMA can occur during I/O cycles.

I/O and sound DMA

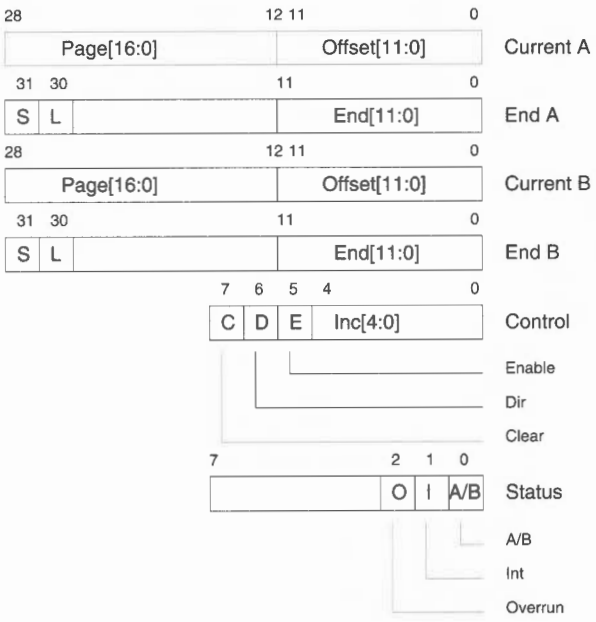
The I/O and sound DMA channels have two sets of pointers, so that data transfers may be 'double buffered' as is the case with the MEMC1a sound DMA channel. The DMA pointers consist of two pairs (A and B) of 29-bit current address registers, and 12 bit end pointers which also have 2 control bits in them. The current and end pointer addresses are inclusive addresses, and the end address is the address of the last transfer, which will depend upon the transfer size. The current address registers are divided into two fields. The lower 12 bits form an offset into a 4K page. The upper 17 bits form a static page number. The end register consists of a 12 bit page offset in the lower 12 bits of the register, and two control bits in the most significant bits of the register. Each channel also has an 8 bit control register, and a three bit status register. The control register is readable and writable, and the status register is read only. Five of the control register bits (Inc[4:0]) control the amount by which the current pointer is incremented after each transfer. Another bit (D) controls the direction of transfer,

and one bit (E) is used to enable and disable the channel. The status bits, and the C bit of the control register are described later.

DMA transfers are constrained to a single physical page by the following mechanism. The bottom 12 bits (page offset) of the current pointer is incremented on each DMA transfer by the programmed increment, and is compared to the bottom 12 bits of the end pointer. The page number is not incremented, and is not compared. This has the effect that it is possible to program the end pointer to be less than the initial page offset, causing the DMA address to wrap around at the end of the page. This is unlikely to be useful.

In order to implement the double buffering mechanism, each pair of registers is used alternately. An interrupt is raised when one of the pair completes its transfer. If the other pair has been programmed by this time, DMA continues using this pair.

Figure 1.3: DMA Address registers (one set per channel)



The increment field in the control register determines the channel increment as follows:

00001	Byte
00010	Half-word
00100	Word
10000	Quad-word

The I/O DMA channels support byte, half-word and word transfers only. The VIDC sound channel can support quad-word DMA, but only when DMA is to VIDC, not when it is from the CODEC. The increment has a different meaning for the video channel (see later).

The direction bit in the control register defines the direction of the DMA transfer. When set, the transfer is from peripheral to memory. Sound channel 0 uses this bit to control whether VIDC sound output mode, or CODEC sound input mode is in use.

Each DMA channel is controlled by a simple state machine. The state machine is able to run when the enable bit is set. The current state is visible in the status register and these bits are read only. The A/B bit indicates which pair of current/end pointers is in use. The Int bit indicates when the channel is requesting an interrupt. The Overrun bit indicates when a channel has stopped because it finished a transfer, and the other pointer pair had not been programmed. Writing a 1 to the C bit of the control register resets the state machine to state 110. The C bit of the control register is self clearing and always reads zero.

The S (Stop) and L (Last) bits in each end register control the behaviour of the channel when transfer of a buffer completes. The S bit must be set if the TC pin is to be asserted at the end of the buffer. The L bit is an indication that the next transfer on that buffer will be the last. It is normally set by IOMD, but must be set by the ARM in the case where the channel is being initialised for a single transfer. For buffers that require more than one transfer, the L bit should be cleared when the end register is written.

In *Figure 1.4* the three bits shown beside each state correspond to the three bits of the status register, and directly reflect the state of the DMA state machine. At reset, the state machine enters state 110. This state and state 111 are the idle states in which no DMA transfers occur. The transition between states occurs either by a buffer finishing, or by the ARM programming the next pointer pair. The current and end pointers must be programmed in that order, as it is the write to the end pointer which actually causes the state transition.

In practice, a complete DMA transaction is performed by a software state machine, as shown in *Figure 1.5*, where N is the buffer number being transferred and LastN is the buffer number of the last buffer to be transferred, which should have the Stop bit set when programmed. When the last buffer has been programmed in, and the next interrupt happens, a dummy value is programmed into the next buffer pair in order to clear the interrupt. The following interrupt happens after the last buffer has been transferred, at which point DMA can be disabled and the channel reallocated. When the Wait for I box is encountered, the software checks the I (Int) bit: if set, it continues to the next step; if clear, the software exits and waits for the next DMA interrupt. After a buffer with the S bit set has been transferred, the hardware always enters one of the idle states; it never continues to the other buffer. The scheme is designed to cope with all possible cases of overrun.

Figure 1.4: Hardware DMA state machine diagram

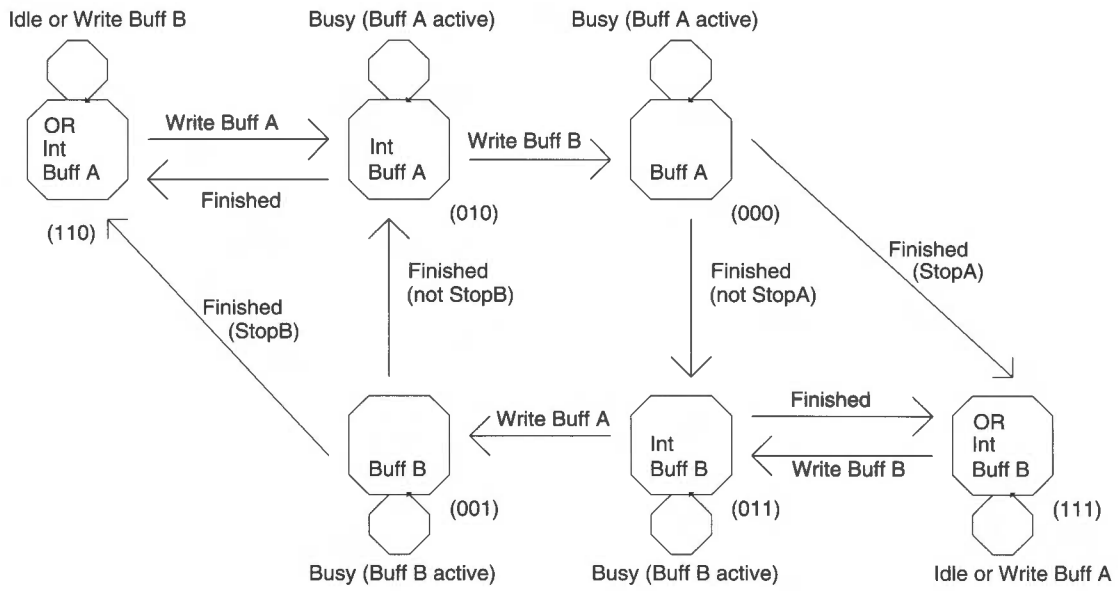
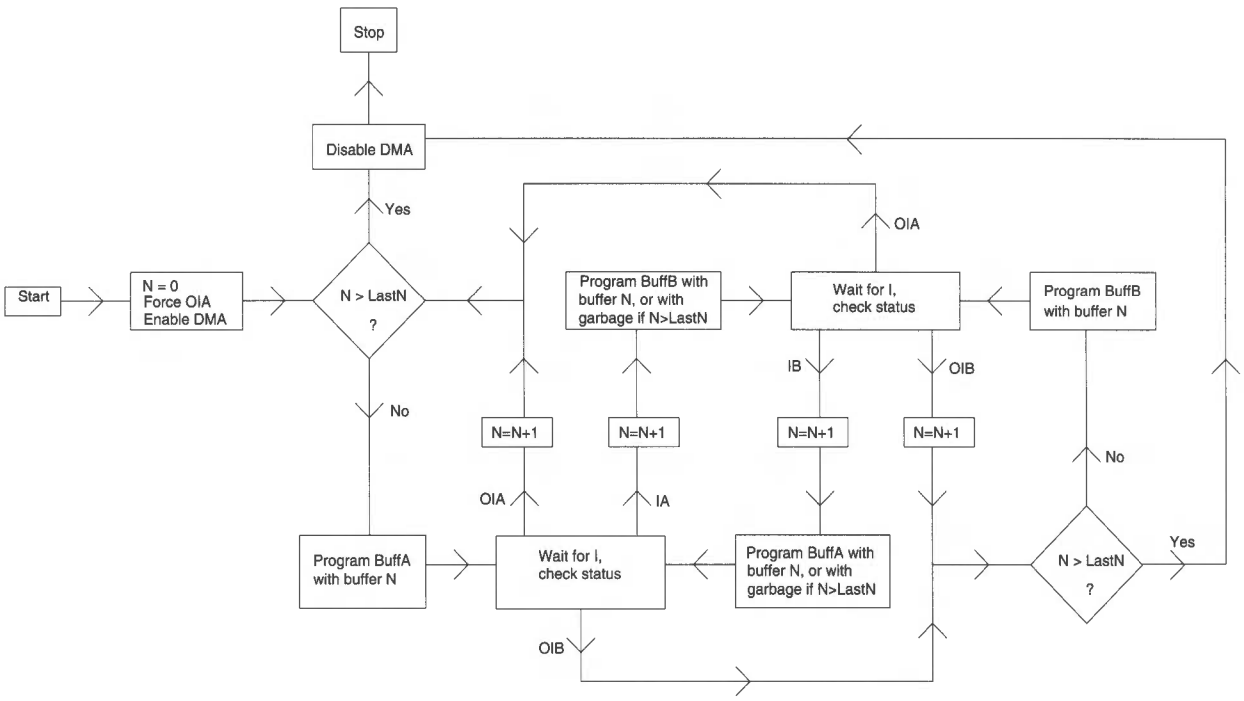


Figure 1.5: Software DMA state machine diagram

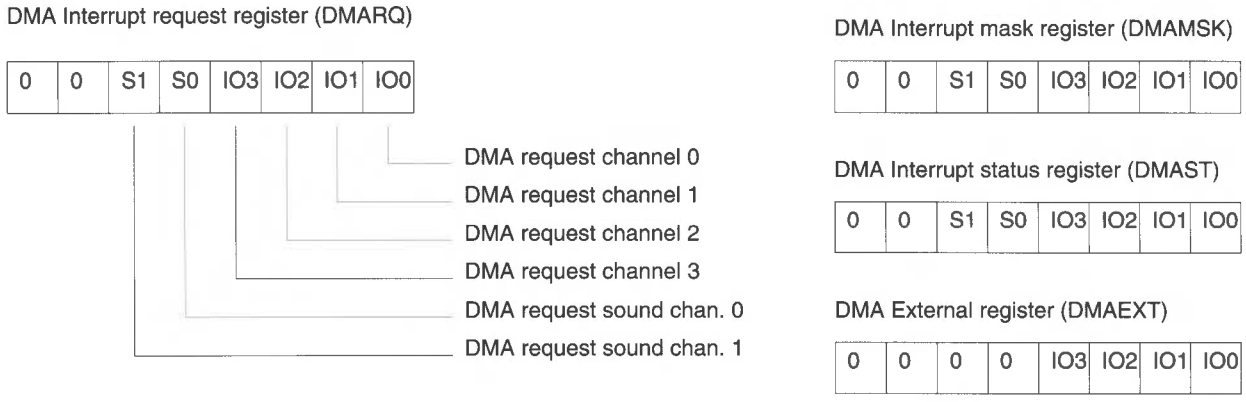


Additionally there is a set of interrupt registers for the DMA channels. For each channel there is a mask bit, a status bit, and a request bit, the status bit being a replication of the I bit in the DMA state machine. There are 6 interrupting DMA channels in total, and the interrupt registers are arranged such that there is a DMA channel per bit of each register, with 2 bits per register spare, as shown in *Figure 1.6*.

In *Figure 1.6*, the DMA interrupt status register indicates which channels have interrupts outstanding. A channel generates an interrupt when it reaches the end of the current buffer. An interrupt will be generated if the relevant DMA interrupt mask is enabled. The DMA request register holds the logical AND of the DMA interrupt status and DMA interrupt mask registers, indicating which channels are requesting an interrupt.

When using, for example, an 8-slot backplane where the data lines are buffered by a '245 device or similar on the backplane, IOMD provides an output enable signal ($\overline{\text{PBOE}}$) which can be programmed to be active or inactive during DMAs from peripheral to memory. In this way the '245 buffer can be disabled for DMAs from 'internal' peripherals, such as the Network card, or enabled for DMAs from 'external' peripherals on expansion cards. To do this, the DMAEXT register is used. Bits 3:0 of the DMAEXT register map to I/O DMA channels 3 to 0, and setting the relevant bit to a 1 indicates that the peripheral is external. There are no DMAEXT bits for the sound DMA channel, as the sound CODEC is always an on-board peripheral.

Figure 1.6: DMA Interrupt registers



Registers

The following table lists the registers in IOMD. The physical base address of these registers is &0320 0000, the same as the address of the IOC internal registers in previous platforms. The size field indicates the width of the register, although some bits may not be used in a register.

Table 1.3: Register definitions

Name	Address	Size	Read	Write	Function	Reset state
IOCR	0	(8)	Status	Control	I/O control	-1-
KBDDAT	4	(8)	Rx Data	Tx Data	Keyboard data	-x-
KBDCR	8	(8)	Status	Control	Keyboard control	-0-
IRQSTA	10	(8)	Status	---	IRQA status	
IRQRQA	14	(8)	Request	Clear	IRQA request/clear	-x-
IRQMSKA	18	(8)	Mask	Mask	IRQA mask	-0-
IRQSTB	20	(8)	Status	---	IRQB status	
IRQRQB	24	(8)	Request	---	IRQB request	
IRQMSKB	28	(8)	Mask	Mask	IRQB mask	-0-
FIQST	30	(8)	Status	---	FIQ status	
FIQRQ	34	(8)	Request	---	FIQ request	
FIQMSK	38	(8)	Mask	Mask	FIQ mask	-0-
T0LOW	40	(8)	Count Low	Latch Low	Timer 0 low bits	-x-
T0HIGH	44	(8)	Count High	Latch High	Timer 0 high bits	-x-
T0GO	48	(8)	---	Go command	Timer 0 Go command	-x-
T0LAT	4C	(8)	---	Latch command	Timer 0 Latch cmd	-x-
T1LOW	50	(8)	Count Low	Latch Low	Timer 1 low bits	-x-
T1HIGH	54	(8)	Count High	Latch High	Timer 1 high bits	-x-
T1GO	58	(8)	---	Go command	Timer 1 Go command	-x-
T1LAT	5C	(8)	---	Latch command	Timer 1 Latch cmd	-x-
ROMCR0	80	(8)	RomCr0	RomCr0	ROM control bank 0	-0-
ROMCR1	84	(8)	RomCr1	RomCr1	ROM control bank 1	-0-
DRAMCR	88	(8)	DramCr	DramCr	DRAM control	-0-
VREFCR	8C	(8)	VrefCr	VrefCr	VRAM & refresh control	-0-
FSIZE	90	(8)	Size	Size	Flyback line size	-x-
ID0	94	(8)	ID0	---	Chip ID no. low byte	
ID1	98	(8)	ID1	---	Chip ID no. high byte	
VERSION	9C	(8)	Version	---	Chip version number	
MOUSEX	A0	(16)	MouseX	MouseX	Mouse X position	-x-
MOUSEY	A4	(16)	MouseY	MouseY	Mouse Y position	-x-
DMATCR	C0	(8)	DmaTcr	DmaTcr	DACK timing control	-x-
IOTCR	C4	(8)	IoTcr	IoTcr	I/O timing control	-x-
ECTCR	C8	(8)	EcTcr	EcTcr	Expansion card timing	-x-

Table 1.3: Register definitions

Name	Address	Size	Read	Write	Function	Reset state
DMAEXT	CC	(8)	DmaExt	DmaExt	DMA external control	-x-
IO0CURA	100	(32)	IO0CurA	IO0CurA	I/O DMA 0 CurA	-x-
IO0ENDA	104	(32)	IO0EndA	IO0EndA	I/O DMA 0 EndA	-x-
IO0CURB	108	(32)	IO0CurB	IO0CurB	I/O DMA 0 CurB	-x-
IO0ENDB	10C	(32)	IO0EndB	IO0EndB	I/O DMA 0 EndB	-x-
IO0CR	110	(8)	IO0Control	IO0Control	I/O DMA 0 Control	x0000000
IO0ST	114	(8)	IO0Status	---	I/O DMA 0 Status	xxxxx110
IO1CURA	120	(32)	IO1CurA	IO1CurA	I/O DMA 1 CurA	
IO1ENDA	124	(32)	IO1EndA	IO1EndA	I/O DMA 1 EndA	
IO1CURB	128	(32)	IO1CurB	IO1CurB	I/O DMA 1 CurB	as I/O 0
IO1ENDB	12C	(32)	IO1EndB	IO1EndB	I/O DMA 1 EndB	
IO1CR	130	(8)	IO1Control	IO1Control	I/O DMA 1 Control	
IO1ST	134	(8)	IO1Status	---	I/O DMA 1 Status	
IO2CURA	140	(32)	IO2CurA	IO2CurA	I/O DMA 2 CurA	
IO2ENDA	144	(32)	IO2EndA	IO2EndA	I/O DMA 2 EndA	
IO2CURB	148	(32)	IO2CurB	IO2CurB	I/O DMA 2 CurB	as I/O 0
IO2ENDB	14C	(32)	IO2EndB	IO2EndB	I/O DMA 2 EndB	
IO2CR	150	(8)	IO2Control	IO2Control	I/O DMA 2 Control	
IO2ST	154	(8)	IO2Status	---	I/O DMA 2 Status	
IO3CURA	160	(32)	IO3CurA	IO3CurA	I/O DMA 3 CurA	
IO3ENDA	164	(32)	IO3EndA	IO3EndA	I/O DMA 3 EndA	
IO3CURB	168	(32)	IO3CurB	IO3CurB	I/O DMA 3 CurB	as I/O 0
IO3ENDB	16C	(32)	IO3EndB	IO3EndB	I/O DMA 3 EndB	
IO3CR	170	(8)	IO3Control	IO3Control	I/O DMA 3 Control	
IO3ST	174	(8)	IO3Status	---	I/O DMA 3 Status	
SD0CURA	180	(32)	SD0CurA	SD0CurA	Sound DMA 0 CurA	
SD0ENDA	184	(32)	SD0EndA	SD0EndA	Sound DMA 0 EndA	
SD0CURB	188	(32)	SD0CurB	SD0CurB	Sound DMA 0 CurB	as I/O 0
SD0ENDB	18C	(32)	SD0EndB	SD0EndB	Sound DMA 0 EndB	
SD0CR	190	(8)	SD0Control	SD0Control	Sound DMA 0 Control	
SD0ST	194	(8)	SD0Status	---	Sound DMA 0 Status	
SD1CURA	1A0	(32)	SD1CurA	SD1CurA	Sound DMA 1 CurA	
SD1ENDA	1A4	(32)	SD1EndA	SD1EndA	Sound DMA 1 EndA	
SD1CURB	1A8	(32)	SD1CurB	SD1CurB	Sound DMA 1 CurB	as I/O 0
SD1ENDB	1AC	(32)	SD1EndB	SD1EndB	Sound DMA 1 EndB	
SD1CR	1B0	(8)	SD1Control	SD1Control	Sound DMA 1 Control	
SD1ST	1B4	(8)	SD1Status	---	Sound DMA 1 Status	
CURSCUR	1C0	(32)	CursCur	CursCur	Cursor DMA Current	-x-
CURSINIT	1C4	(32)	CursInit	CursInit	Cursor DMA Init	-x-
VIDCUR	1D0	(32)	VIDCur	VIDCur	Video DMA Current	-x-

Table 1.3: Register definitions

Name	Address	Size	Read	Write	Function	Reset state
VIDEND	1D4	(32)	VIDEnd	VIDEnd	Video DMA End	-x-
VIDSTART	1D8	(32)	VIDStart	VIDStart	Video DMA Start	-x-
VIDINIT	1DC	(32)	VIDInit	VIDInit	Video DMA Init	-x-
VIDCR	1E0	(8)	VIDControl	VIDControl	Video DMA Control	xx000000
DMAST	1F0	(8)	Status	---	DMA interrupt status	
DMARQ	1F4	(8)	Request	---	DMA interrupt request	
DMAMSK	1F8	(8)	Mask	Mask	DMA interrupt mask	-0-

Reset and power-on reset

IOMD has an active high power on reset input, with Schmitt level input, and a bidirectional active low reset pin. The reset pin is driven low during power on reset, and may be pulled low at any time to reset the chip. The ID I/O bit is driven low during reset. The POR bit in the IRQA interrupt register is set on power on reset. The JTAG interface is reset by an internal power on reset cell in IOMD.

During reset, Nfiq becomes an input and taking it low invokes test features. Nfiq should be pulled up by an external pull-up resistor.

I²C and RTC

The primary use of the I²C bus is to enable the CPU to talk to the PCF 8583, a combined battery-backed real time clock (RTC) and the CMOS RAM IC. The bus is also tracked to the expansion bus.

The I²C bus is a two-wire bus specified by Philips. The two signals are clock and data, both of which are of the open collector type with a 4k7 pull-up.

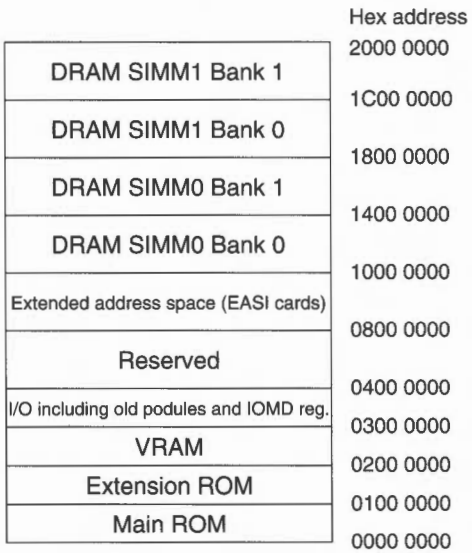
The CPU controls the bus by writing (& reading) to the I/O control register in IOMD (address &0320 0000), bit 0 = data, bit 1 = clock. Note that the higher bits in this register are used to control other functions. The appropriate operating system calls (see *RISC OS 3 Programmer's Reference Manual*) should be used to read or write to devices on I²C bus.

A 1.2V rechargeable cell is used to provide the battery back-up. This is trickle charged from the +5v supply when the computer is on.

Memory system

The system physical memory map is shown below. For the purposes of DMA, the VRAM appears in the whole of the bottom half of the address space, as bit 28 of the DMA address selects between DRAM and VRAM in this implementation. The total memory map is 512MBytes, as only 29 address bits from the ARM are connected to IOMD. However, this does not prevent future platforms having a larger physical memory map.

Figure 1.7: Risc PC System Memory map



Since each SIMM may have one or two banks on it, and as each bank will usually be less than 64MB, the physical DRAM address map may be discontiguous.

I/O address space

The I/O address space beginning at 0300 0000 is allocated as shown in the I/O section and the podule address space is the same as in previous platforms. However, the Extended Address Space interface allocates 16MB per card.

There are two types of peripheral access supported by IOMD. PROG address space is accessed with fixed timing and the access cycles are not divisible by DMA. True I/O address space accesses may be interrupted by non I/O DMA. The IOMD internal PROG address space is from 0320 0000 to 0324 0000 and this includes all IOMD internal registers. There is also an external PROG address space from 0340 0000 to 037F FFFF. Accesses to 0340 0000 to 035F FFFF activate the Nprog pin. Accesses to addresses from 0360 0000 to 037F FFFF do not activate the Nprog pin. This area is intended for OPEN Bus second bus master system registers. Accesses to addresses in the range 0350 000 to 035F FFFF and 0370 0000 to 037F FFFF arbitrate for the memory bus on quad word boundaries, and do not arbitrate for the VIDC programming bus first. Accesses in the range 0340 0000 to 034F FFFF and 0360 0000 to 036F FFFF arbitrate for the memory bus on every accesses, and arbitrate for the VIDC data bus first. Thus VIDC should be programmed at location 0340 0000, as this activates the Nprog pin, and arbitrates for the VIDC programming bus at the start of the cycle.

True I/O address space is from 0300 0000 to 0400 0000 excluding those areas which are mapped to PROG space as detailed above. There is also another area of I/O space from 0800 0000 to 1000 0000. The I/O address map is detailed in the section *DEBI Expansion I/F* on page 1-19.

Accesses to SIO space in the S1 to S3 area are assumed to be internal peripherals by IOMD, and will not assert the $\overline{\text{PBOE}}$ signal on a read, and accesses to SIO space in the S4 to S7 area are assumed to be external peripherals, and will thus assert the $\overline{\text{PBOE}}$ signal. The $\overline{\text{PBOE}}$ signal is always asserted when not reading.

RAM control

IOMD will directly control two standard 32-bit wide, 72-pin SIMMS. Each SIMM has one or two RAS lines, and 4 CAS lines, one for each byte in the word. Thus, IOMD has 4 RAS lines and 4 CAS lines in total. In addition, IOMD directly supports VRAM, and there is an additional RAS line to select the VRAM

There are 12 RA address lines, and 3 control bits to control address multiplexing options, meaning there are 8 possible options, of which 4 are considered useful, as shown below. The most significant bit of the DRAM size control is only applicable for VRAM, and is therefore not present for DRAM, and is assumed by the hardware to be zero.

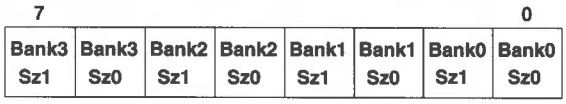
Table 1.4: CAS/RAS mapping

RA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0	
Size 000 (Size 00 for DRAM)													
PA row	25	23	21	20	19	18	17	16	15	14	13	12	1M, 4M, and 16M DRAM & 1 bank 1M VRAM
PA col	24	22	11	10	9	8	7	6	5	4	3	2	
Size 001 (Size 01 for DRAM)													
PA row	25	23	21	11	19	18	17	16	15	14	13	12	256K DRAM & 1 bank 256K VRAM
PA col	24	22	11	10	9	8	7	6	5	4	3	2	
Size 010													
PA row	25	23	21	20	19	18	17	16	15	14	13	12	2 bank VRAM (256K)
PA col	24	22	12	11	10	9	8	7	6	5	4	3	
Size 110													
PA row	25	23	21	20	19	18	17	16	15	14	13	22	2 bank VRAM (1M)
PA col	24	22	12	11	10	9	8	7	6	5	4	3	

A[27:26] are decoded to select the DRAM bank, and hence the appropriate RAS line. This means that the physical memory map may be discontiguous if each bank does not contain the maximum 64MB. Normally, the VRAM used will be 256Kx32, or 256Kx64, with the two banks interleaved on a word basis on the DRAM interface side (see video interface section).

An 8-bit register (DRAMCR) is provided to control the DRAM row address options and is shown below. Four pairs of two bits control the DRAM row address mapping for each RAM bank. Another control register (VREFCR) is used to control the VRAM column address options which will vary depending on whether one or two megabytes of VRAM are fitted. The VRAM control register also contains the refresh timing information, and is shown in *Figure 1.11* on page 1-13. The format of the DRAM control register is shown in *Figure 1.8*. The DRAMCR is reset to zero when IOMD is reset.

Figure 1.8: DRAM Control Register



DRAM (and VRAM) control and timing is controlled by a state machine running at 32MHz. The DRAM interface supports page-mode DRAMs. S-cycles run at 16MHz, and N-cycles take 2.5 times the S-cycle time, i.e. they run at 6.4MHz. This means that S-cycles take 2 cycles of the 32MHz clock, and N-cycles take 5 cycles of the 32MHz clock. An example DRAM timing waveform is shown in *Figure 1.9*. Note that the **CAS** signal is delayed by half a 32MHz clock cycle for a write, to allow more set up time for data into the RAM. The column address is also delayed by half a 32MHz clock cycle during writes, in order to ensure that there is enough column address hold time.

Figure 1.9: Example DRAM control signals (read)

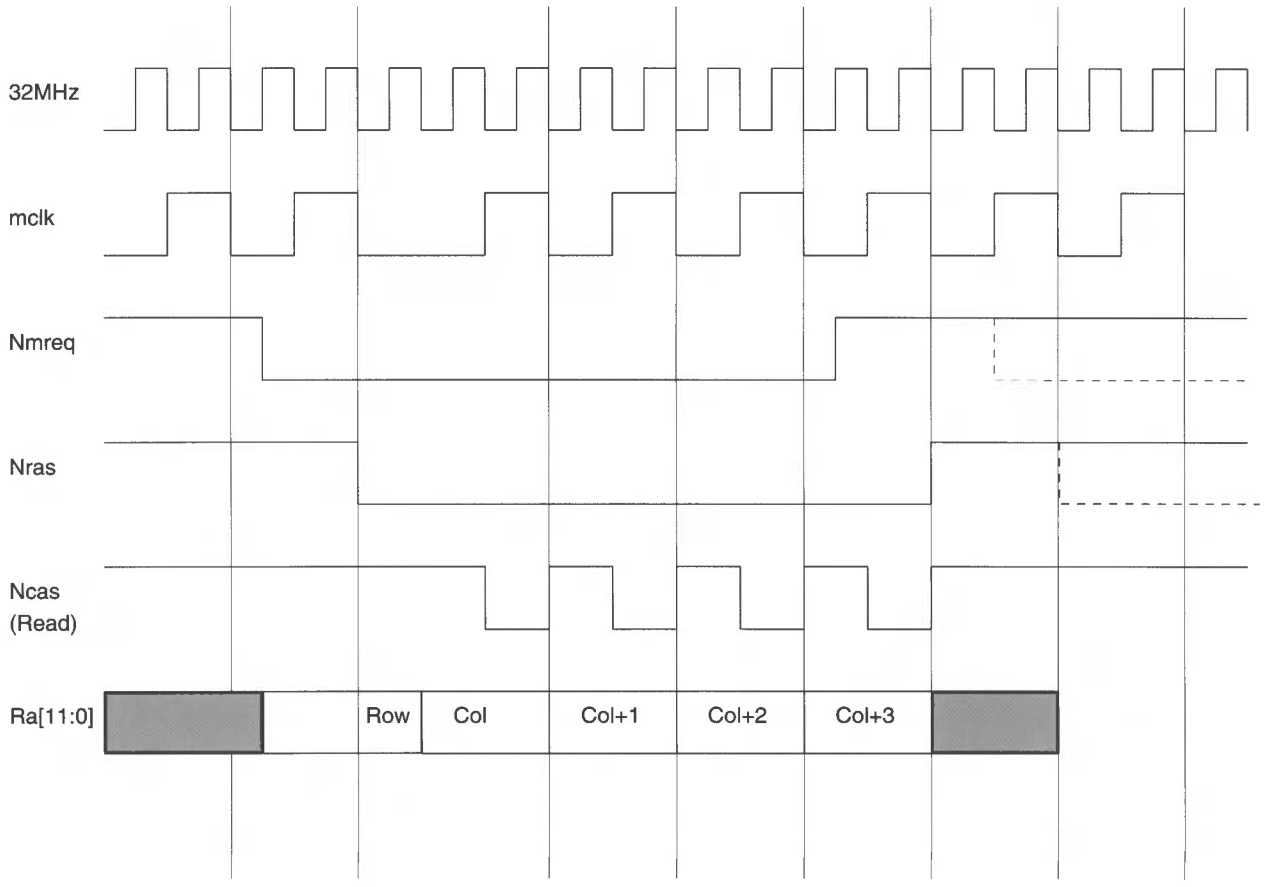
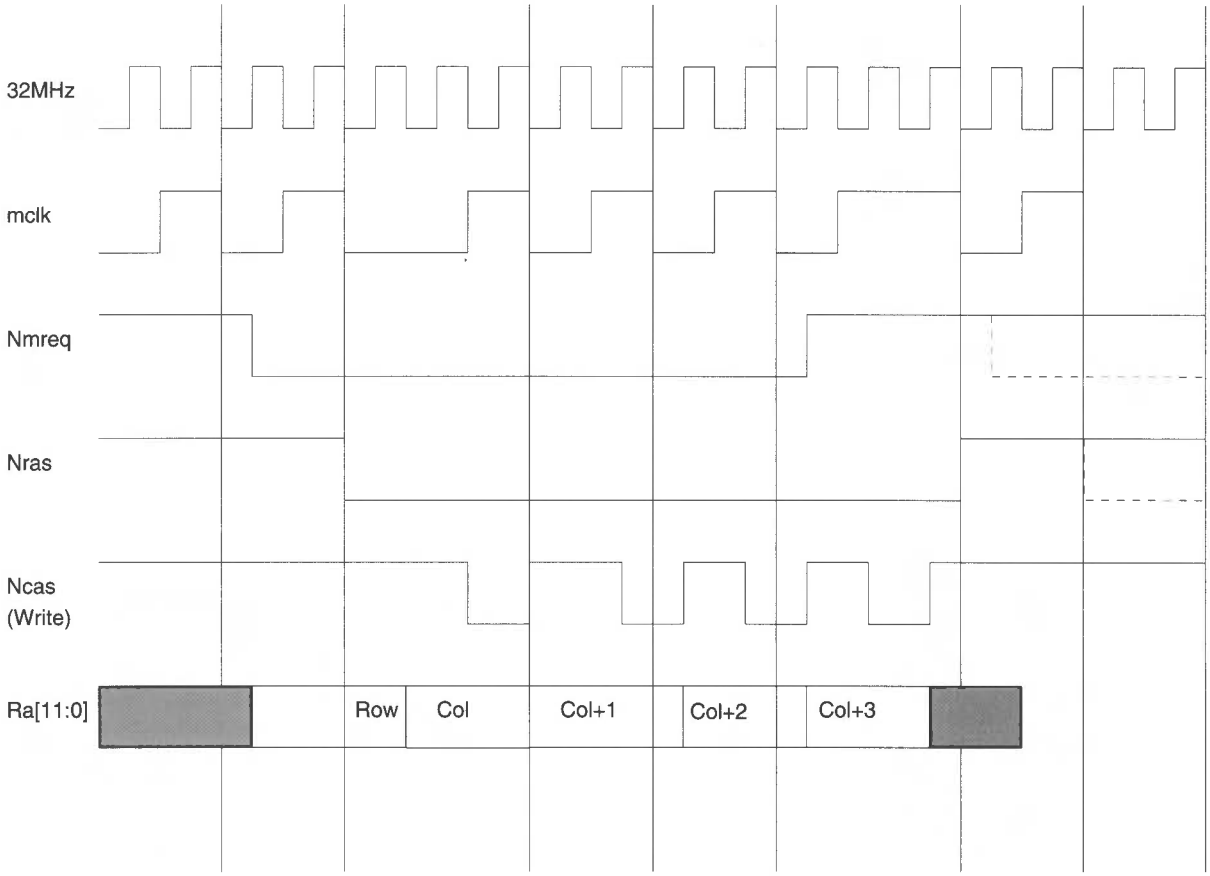


Figure 1.10: Example DRAM control signals (write)



DRAM refresh is performed using CAS-before-RAS refresh. A refresh control register (VREFCR) of which 2 bits are currently defined for refresh operation, is provided to control the refresh rate. This register also contains the VRAM control bits. The register is reset to zero when IOMD is reset. The refresh rate is derived from the reference clock (64MHz), and can be set to 16 or 128µS, or disabled. Unused bits in this register should be written to 0, but their state is undefined when read, including after reset. Thus bits 4, 2 and 1 are all undefined on a read. DRAM refreshes are staggered by IOMD, to minimise the instantaneous power consumption required.

Figure 1.11: VRAM and Refresh Control Register (VREFCR)

7							0
VRAM Sz2	VRAM Sz1	VRAM Sz0	0	Rate 3	Rate 2	Rate 1	Rate 0

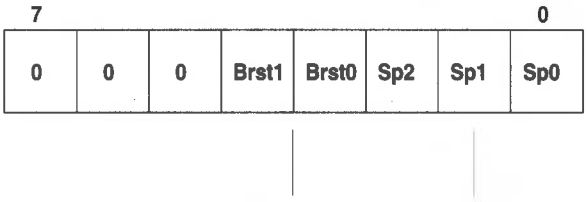
0000 = Refresh off
0001 = 16uS
1000 = 128uS
All other values undefined

ROM control

IOMD will support two 16MB banks of ROM with individually controllable timing parameters. The access time can be varied from around 220nS downwards in steps of 31.25nS. In addition, support is provided for burst mode ROMs which allow rapid access to sequential addresses controlled by A0 and A1. Five control bits per bank are used to control these parameters. Three bits control the basic access speed, and two bits control whether burst is used and the burst access speed. In burst mode, subsequent accesses are shorter than the initial access time. There are two ROM control registers, one for each ROM bank, with the bit allocation as shown in the diagram below. The ROM control registers (ROMCR0 and ROMCR1) are reset to zero when IOMD is reset. Unlike machines based on MEMC1A, IOMD allows writes to be made to the ROM areas. The ARM MMU should be programmed to prevent writes to the ROM space if the ROM area does not contain writable memory such as SRAM.

During sequential accesses to ROM, Nromcs will stay low, and the ARM addresses change. Thus Nromcs is a combinatorial signal, and a falling edge on it cannot be relied upon. The timing of Nromcs is the same for reads and writes. Nromcs typically rises 0 to 5 nS before mclk falls at the end of the cycle.

Figure 1.12: ROM Control Register, one per ROM bank (ROMCR0 & ROMCR1)



Burst speed	Initial speed
00 = Burst off	000 = 218.75nS
01 = 125nS	001 = 187.5nS
10 = 93.75nS	010 = 156.25nS
11 = 62.5nS	011 = 125nS
	100 = 93.75nS
	101 = 62.5nS

Video and audio system

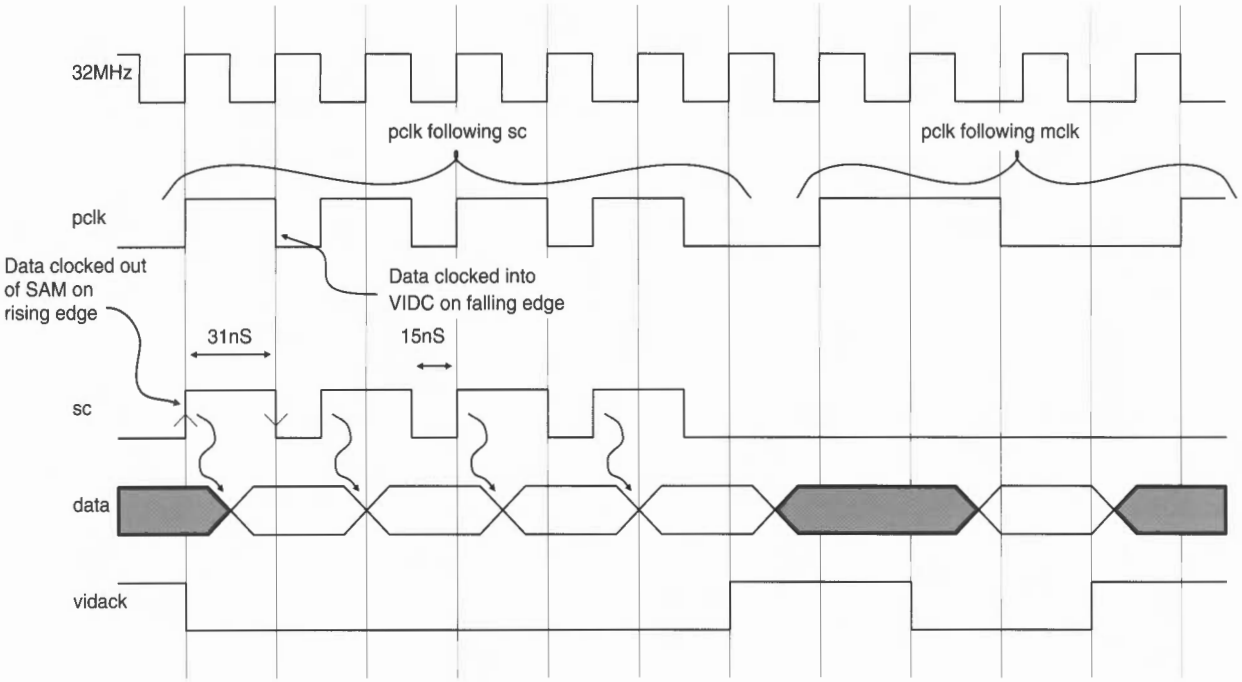
VIDC20 Video interface

The video system supports 1 or 2 MB of VRAM, but will also work with DRAM. VIDC is used in 32 bit DRAM interface mode for DRAM or one bank of VRAM (1MB) and 64 bit DRAM interface mode for two banks of VRAM (2MB). Cursor, sound and programming information come from the main data bus, as does the video data when VRAM is not used. When used, the VRAM serial ports connect directly to VIDC's data input ports with the main data bus isolated from the lower 32 bit SAM data port by four 74ACT244 buffers controlled by an active low output enable signal (Ncdoe) generated by IOMD. During cursor DMA (horizontal retrace time), programming and sound DMA the VRAM serial port is also disabled. When both banks of VRAM are fitted, nWE and nOE (or DT) are used to interleave the VRAM banks' data busses onto the main system data bus on a word basis, using A[2] to select the required bank.

At the start of each frame, IOMD does a full transfer to the VRAM, to initialise the video pointer in the SAM. It then does split transfers whenever needed, as indicated by the qsf pin of the VRAM. The full transfer is done on the last but one line of the flyback period. This is to ensure that the VRAM serial port is loaded with new data if the frame buffer has been updated during flyback. To do this, IOMD counts the flyback lines, and when the last line but one is reached, it does the transfer. The 8 bit FSIZE register in IOMD is programmed with the number of flyback lines minus 1.

The VRAM serial ports are clocked at 21.33MHz using a 'bursty' clock. When VIDC20 asserts vidrq the response from IOMD is to assert vidak and to clock the VRAM serial port clock sc four times. The VRAM serial clock is derived from the 64MHz reference clock by dividing by 3, such that the clock is high for 2 64MHz periods, and low for one 64MHz period. Data is clocked out of the VRAM serial port on the rising edge of sc and is clocked into VIDC on the falling edge of pclk, which is the same as sc during video data transfers (see *Figure 1.13*). pclk is the same as mclk during cursor, programming and sound transfers. A change on the qsf output from the VRAM indicates that a transfer cycle is required. The current video pointer VCUR is then incremented by the split port SAM length, and a transfer cycle is requested to the main bus arbiter.

Figure 1.13: VRAM clock signals



Using a 21.33MHz interface to VIDC gives a theoretical peak bandwidth from the frame buffer to the display of 85.33MB/sec for a 1MB VRAM machine using a 32-bit interface, and 170.66MB/sec for a 2MB VRAM machine, using the 64 bit interface. However, in practice the overall system bandwidth requirements mean that the sustained best case maximum is 80 MB/sec and 160 MB/sec respectively and in order to provide a safety margin, the bandwidth limit file stored in the !Boot directory on the hard disc sets the maximum bandwidths to 76 MB/sec and 152 MB/sec respectively.

Cursor DMA

The cursor DMA channel is controlled by two 29 bit registers: init and current. Data is transferred from the current register address in quad words under control of: vidrq, vidak and vnc. The init register is copied to the current register during flyback. There is no control register for this channel and hence no interrupts may be generated. It is enabled and disabled with the video transfer channel. Cursor data can be held in either VRAM or DRAM. The format of the cursor registers is shown in the IOMD register definition section.

Video DMA

The video transfer channel is similar in structure to that of the older MEMC1a device used in previous platforms and is controlled by start, end, init and current registers which are all 32 bits wide. Please refer to the section on IOMD for a list of all IOMD's registers.

VIDStart is programmed with the address of the start of memory used for the screen buffer and VIDEnd is programmed with the address of the last transfer of the video buffer memory. Thus it equals the address of the end of the video buffer, minus the transfer size, i.e. quad word (16 bytes) in DRAM mode or the half-SAM length in VRAM mode. One bank of 1Mbyte VRAM made up from 4 off 2Mbit (256K*8) VRAMs has a half-SAM length of 1*4*512/2=1024 bytes. Two banks have a half-SAM length of 2*4*512/2 = 2048 bytes.

The addresses for the start and end of the video buffer memory have the following restrictions on their values:

- They must lie within the bounds of a single16MB aligned block in the physical address space.
- In DRAM mode they must each be on a quad word boundary

- In VRAM mode, they must each be on a half-SAM boundary and the buffer size must be a multiple of 2 times the half-SAM length (i.e. N*4096 bytes for 2 banks of VRAM and N*2048 for the 1 bank case).

Note the VIDStart and VIDEnd values written to IOMD will always differ by an odd number of half-SAM lengths in VRAM mode due to VIDEnd being programmed with the screen memory end address less the half-SAM length as mentioned above.

The video init (VIDInit) register is programmed with the address of the start of the screen data to be displayed, i.e. the address of the first pixel in the frame. This address must be a multiple of N bytes where N is 16 (i.e. 4 words) in DRAM mode, 8 (2 words) on 2 bank VRAM machines, and 4 (1 word) on 1 bank VRAM machines. It is recommended that addresses are aligned to 16 byte boundaries to ensure compatibility with all possible video configurations. However, finer address resolution in VRAM modes would allow, for example, finer horizontal scrolling to be performed in certain specialist applications.

NB Older platforms based on MEMC1/VIDC1 also have alignment restrictions of 16 bytes on VIDInit.

During flyback, the current register, VIDCur, is initialised to VIDInit. VIDCur then increments by Inc (VIDCR[4:0]) until either the end of the frame data, or the end of the video buffer area is reached. In the latter case VIDCur is reloaded with the value in VIDStart, and continues to increment from there, i.e. the data for the frame is wrapped around within the physical memory area defined by VIDStart and VIDEnd. This mechanism allows for efficient vertical scrolling of the video display.

Video address incrementing

The video transfer DMA channel in IOMD generates the VRAM transfer addresses and is designed to use VRAMs with split SAM ports. On each split transfer, one half of the SAM is loaded with new data and so the video increment is the half SAM length. The video start and end addresses must therefore be on half-SAM boundaries.

If the VIDInit register is equal to or greater than the VIDEnd register, implying the frame start address is somewhere in the last half-SAM of the video buffer, then the video last bit in the VIDInit register will need to be set manually. This is because the comparison as to whether a transfer is the last in the buffer is always done during a video transfer cycle, for the next video transfer cycle.

In VRAM mode, bits 7:0 of the video address are not compared when checking VIDCur against VIDEnd. The number of bits compared depends upon the value programmed into Inc, if programmed to 1, meaning 256 bytes, then all of bits 23:8 are compared, if 2 (512 bytes), bits 23:9 are compared, if 4 only bits 23:10 are compared, and so on. This ensures that the current pointer when compared with the end address, will always match the end address, even if it is not aligned on a half-SAM boundary. Generally, if the increment is 2^N bytes, then bits 23:N will be compared:

Increment in bytes = 2^N = Inc x 256

$N = \log_2(Inc*256) = 8+\log_2(Inc)$, where N is the least significant bit compared.

Note, Inc must always be a power of 2, i.e. there must only ever be one bit set in the increment field in VIDCR.

VIDCur is incremented by the half-length of the SAM port after each transfer. When the VRAM has swapped to the other half of the SAM port, the next transfer cycle is requested by the qsf pin changing state. Transfer cycles consist of single VRAM accesses, with a special combination of control signals applied to the VRAM. The reader is referred to a suitable VRAM datasheet for full SAM transfer cycle details.

Since 4 bytes are transferred at a time in a 1MByte VRAM machine, and 8 bytes are transferred at a time in a 2MByte VRAM machine, the value in the increment field is the half-SAM length (256) multiplied by 4/256 for 1MByte VRAM, or multiplied by 8/256 for a 2MByte VRAM machine. So for 1MByte of VRAM, the video increment is 256 x 4 / 256 = 4 and for 2MByte of VRAM it is 256 x 8 / 256 = 8.

When IOMD is used in DRAM mode it transfers quad words and so Inc is programmed with 16.

Frequency Synthesizer

The Frequency synthesizer which generates the pixel clock for VIDC is based on a Phase Locked Loop (PLL). This consists of three parts; a Voltage Controlled Oscillator (VCO) built around the 74AC04 hex inverter IC32 with suitable feedback components R197 and C141, a Phase Comparator (implemented digitally inside VIDC) and a Loop Filter which is essentially a low pass filter to smooth and integrate the phase comparator output (Pcomp) consisting of R183, R186 and C122. Pcomp appears as shown in *Figure 1.15* and the area above 0V minus the area below 0V when filtered provides an average DC bias voltage to the VCO. The phase comparator will cause the positive Pcomp pulse and therefore the average DC bias voltage to increase slightly if it detects that Vclkin is falling behind Refclk, or decrease slightly if it detects that Vclkin is speeding up over Refclk. By programming the r, v and n registers in VIDC the Pixclk output can be varied anywhere from 8Mz up to in excess of 110 MHz. The comparison frequency is determined by the ratio: 24/2r and the resulting pixel clock is equal to 24 x (v/r) x (1/n) MHz.

The VCO relies on the change in propagation delay of a 74AC04 inverter with supply voltage. However, the variation in propagation delay of these parts with temperature and batch is large and thus an operational safety margin is built in to the circuit. At the time of printing, the values of R197 and C141 around the 74AC04 have been chosen to allow best case operation up to 150 MHz, with machines production line tested to 125 MHz in order to guarantee operation up to 110 MHz. *Figure 1.16* shows the typical VCO output frequency as a function of input voltage.

Figure 1.14: VIDC Phase Comparator Block Diagram

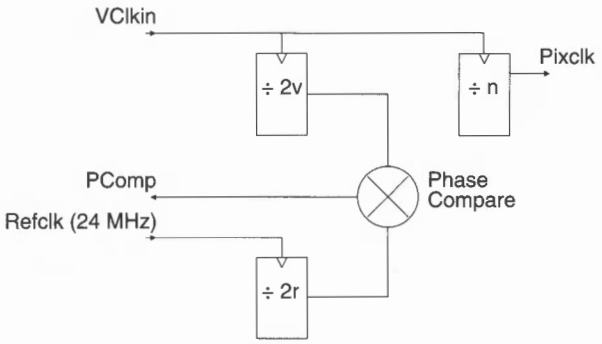


Figure 1.15: Phase Comparator output from VIDC 20

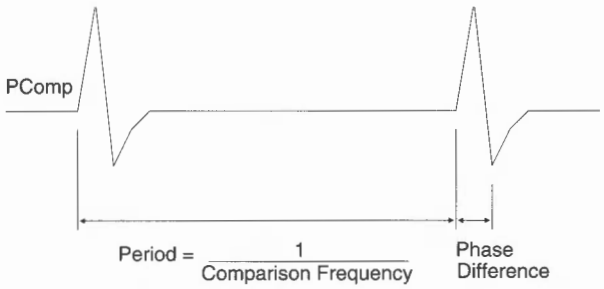
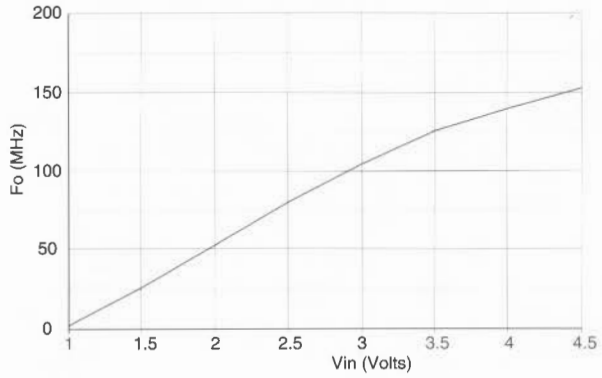


Figure 1.16: VCO frequency against control voltage



Audio & I²S circuitry

The standard sound system is based on the VIDC 1a stereo sound hardware as used in previous platforms. External analogue anti-alias filters are used which are optimised for a 20kHz sample rate. The high quality sound output is available from a 3.5mm stereo jack socket at the rear of the machine which will directly drive personal stereo headphones, or, alternatively, an amplifier and speakers. One internal speaker is fitted, to provide mono audio. When a jack is inserted into the headphone socket the internal speaker is muted.

Two auxiliary audio connectors and a high quality 16 bit Sound output on the main PCB cater for future upgrades (refer to *Interface specifications* on page 2-1 for details).

VIDC sound system hardware

VIDC contains an independent sound channel consisting of the following components: A four-word FIFO buffers 16 8-bit sound samples, with a DMA request issued whenever the last byte is consumed from the FIFO. The sample bytes are read out at a constant sample rate programmed into the 8-bit Audio Frequency Register. This may be programmed to allow samples to be output synchronously at any integer value between 6 and 255 microsecond intervals.

The sample data bytes are treated as sign plus 7-bit logarithmic magnitude and, after exponential digital to analogue conversion, de-glitching and sign-bit steering, are output as a current at one of the audio output pins to be integrated and filtered externally.

VIDC also contains a bank of eight stereo image position registers, each of three bits. These eight registers are sequenced through at the sample rate with the first register synchronised to the first byte clocked out of the FIFO. Every sample time is divided into eight time slots and the 3-bit image value programmed for each register is used to pulse width modulate the output amplitude between the LEFT and RIGHT audio current outputs in multiples of time slot subdivisions. This allows the signal to be spatially positioned in one of seven stereo image positions.

IOMD sound system hardware

Please refer to *I/O and sound DMA* on page 1-4 which describes the operation of both the I/O and Sound DMA channels.

Peripheral control

The PC combo chip provides all the peripheral interfaces: IDE, Serial, Parallel and Floppy, with IOMD providing the keyboard and mouse circuitry. Full details of all these are given in *Interface specifications* on page 2-1.

I/O bus

The I/O bus on the Risc PC is 32 bits wide, of which the lower 16 bits pass through IOMD, and the upper 16 bits are latched and buffered by an external latch. Logic in IOMD is used to position bytes and half words to the appropriate position within the word, for transfer to and from memory. The lower 16 bits from IOMD connect directly to the on-board peripherals, and via a bidirectional buffer to the lower 16 bits of the podule bus. IOMD latches the lower 16 bits of the word, and provides control signals for the external latch and buffer.

The bus supports DMA, and the signals are similar to a cut-down PC-AT bus (i.e. Intel-style control signals, read strobe, write strobe, DACK etc). The bus is clocked at 16MHz, but a number of clock ticks are required for each transfer. In addition, the bus emulates the I/O bus of previous Acorn 32-bit machines. An 8MHz IORQ/IOGT style interface, and the 8MHz 'S-space' interface signals are provided.

I/O Cycle types

There are three types of access timing to the I/O bus, the first two of which are present in MEMC1a/IOC system, and the other one being new to IOMD. The first (8MHz fixed) is the IOC controlled type, in which one of four timings is selected by bits 20:19 of the address. These cycles are based on an 8MHz clock (externally derived clk8). The second type of access (8MHz variable) is also based on an 8MHz clock, and uses the Niorq and Niogt signals, which are referenced to the ref8m pin. The third type of access (16MHz) is referenced to CLK16, the 16MHz I/O clock, and is used for on-board peripherals (e.g. combo), for DACK timing to peripherals using DMA, and for the extended address space expansion cards. The basic timings used for these devices are controlled by the I/O, DMA and expansion card timing control registers (IOTCR, DMATCR, and ECTCR respectively). On-board I/O peripherals such as the combo chip and DMA have four timings available (types A to D), and expansion cards have only two timings available, these being types A and C.

Various different cycle timings may be selected for the 16MHz accesses. These are known as types A to D, where type D is the fastest this has half a 16MHz tick of setup and hold of CS/DACK relative to IOR/IOW and a pulse-width of one 16MHz tick on IOR/IOW. Type C is similar, but has a pulse-width of two 16MHz ticks for IOR/IOW. Type B has one and a half clock ticks of setup and half a tick of hold of CS/DACK to IOR/IOW, and a 3 tick wide IOR/IOW pulse, and type A has one and a half ticks of setup and hold of CS/DACK to IOR/IOW, and a four tick wide IOR/IOW pulse. Their timings are shown in *Table 1.7* on page 1-24. Expansion cards have only timings A and C available to them. The fastest two types reduce the minimum CS/DACK width to one tick for DMA, whilst keeping it 2 ticks for programmed I/O. The slower two timings have a minimum of 2 ticks high for both CS and DACK.

The point at which the DMA request must go away to ensure that another DMA does not happen varies depending upon whether the DMA is a read or a write, and upon the relative phase of rclk and clk16 at the time. For reliability, however, it is recommended that DREQ is removed by the time DACK rises again.

Expansion and I/O system

DEBI Expansion I/F

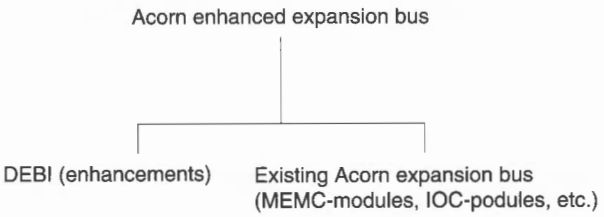
This section is a record of the Acorn enhanced expansion bus implemented specifically in the Risc PC. All details are product specific and all figures and timing information contained in this document should be used for information only.

Important note: Do **not** use this information directly for the design of interface cards. The *Acorn Enhanced Expansion Card Specification* (Part No. 0472,200) should be referred to for design purposes.

Acorn enhanced expansion bus on the Risc PC

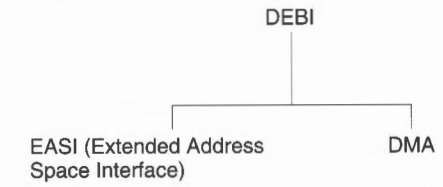
The Acorn enhanced expansion bus breaks down into two parts:

- Enhancements to the existing Acorn expansion bus, which are collectively known as the DMA Extended Bus Interface (DEBI).
- The existing Acorn expansion bus itself, which consists of support for all interface cards using existing Acorn I/O techniques, for example MEMC modules and IOC podules. Although the enhanced expansion bus implemented on the Risc PC supports existing I/O hardware it should be noted that only cards conforming to the single Eurocard dimensions will physically fit inside the Risc PC.



DEBI (DMA Extended Bus Interface)

This is the name given to the 'enhanced' part of the expansion bus which is supported on the Risc PC machines. It includes the new Extended Address Space Interface (EASI) and the capability for 8, 16 or 32 bit wide DMA.



EASI – Extended Address Space Interface

The Extended Address Space Interface (EASI) forms part of the DEBI. The major features of the EASI are:

- 32 bit data bus allowing byte, half-word and word wide transfers
- Additional 16MB of address space per expansion slot
- Choice of two access cycle times
- Up to 6 MB/second transfer rate
- Intel compatible control signals

It is anticipated that all future expansion cards shall be of the single Eurocard form factor. This will enable card guides to be provided and improve the EMC qualities of the enclosure.

DMA – Direct Memory Access

The DEBI interface on the Risc PC supports four DMA channels. These are tracked to the backplane socket on the Risc PC motherboard but only two channels are intended for general use. These two 'general purpose' DMA channels are DRQ2 and DRQ3 from IOMD, and are tracked up the backplane and routed to slots 0 and 1. The DRQ1 channel is reserved for use on board (for internal purposes), and the DRQ0 channel is used for the network card.

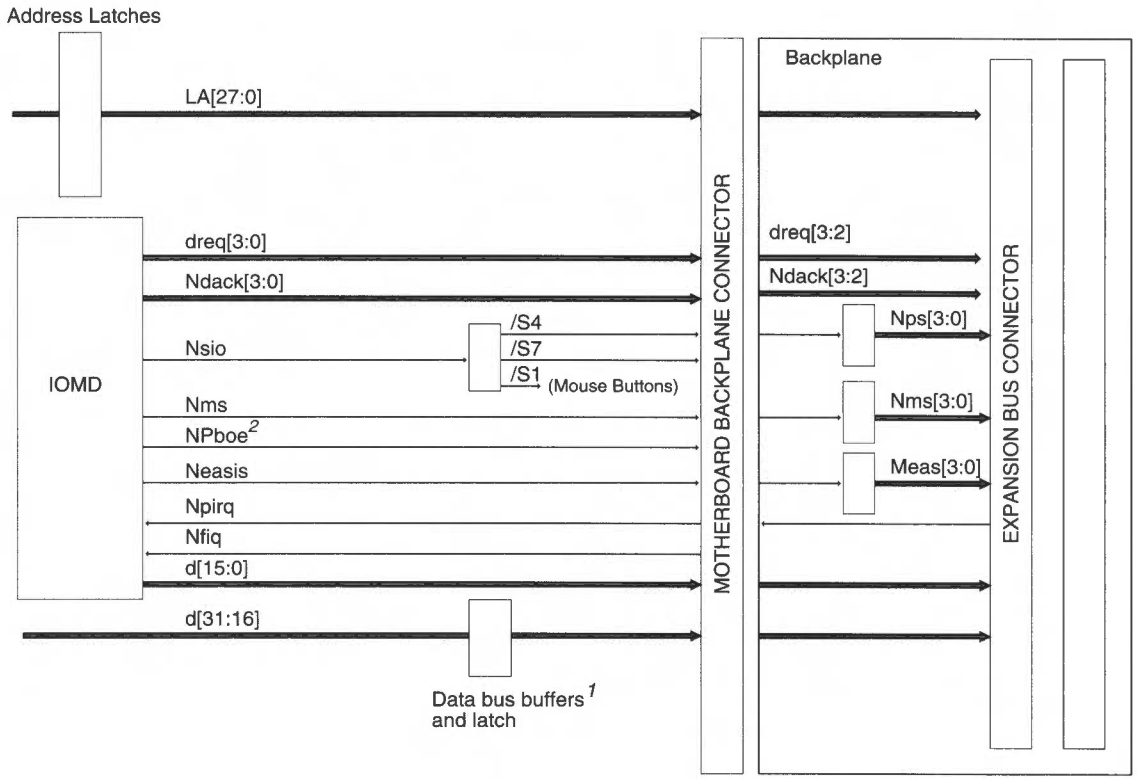
The DMA transfers may be 8, 16 or 32 bits wide. A full description of how DMA is used and programmed is beyond the scope of this document and can be found in the *RISC OS 3 Programmer's Reference Manual.*

General architecture

Figure 1.17 shows how the Enhanced Expansion Bus fits into the Risc PC main system architecture.

All address lines are latched before being sent to the expansion bus. Data lines going to the backplane are split into two with the lower sixteen bits being buffered through IOMD and the upper 16 bits being buffered through external latches. Upper 16 data bits are only used for word wide DMA and EASI read/writes. IOMD performs all byte steering required on the lower 16 data bits in order to transfer data to and from the machine core to support the different interface types.

Figure 1.17: Connections to Risc PC main architecture



The hardware implementation of the Risc PC expansion bus driver circuitry is contained inside IOMD. All I/O space is mapped into the main system memory map and control registers are used to select cycle types, determine bus interrupt status and initialise DMA transfers. Control registers are located inside IOMD. Details of the control registers are given in *Control register definitions* on page 1-23. The I/O memory map is shown in *I/O memory map* on page 1-24 and the overall system memory map appears elsewhere in this manual.

Notes:

1 The upper 16 data lines d[31:16] are driving at all times except during DMA and Easi space reads. Consequently any expansion card with data bus buffers connected to the upper sixteen data bits should not enable them for output except during extended address space and DMA reads.

2 $\overline{\text{PBOE}}$ – Peripheral Bus Output Enable (active low). $\overline{\text{PBOE}}$ is driven by IOMD. It is tracked to the backplane slot on the Risc PC but not used on 2- or 4-slot backplanes. Its purpose is to provide a control signal to enable data buffers for use on larger backplanes (i.e. any backplane with more than four slots).

$\overline{\text{PBOE}}$ during all I/O Reads and Writes is always low (i.e. active) except for the following cases:

- During internal S-space reads, therefore peripheral devices should be aware that when using an 8 slot backplane (utilizing $\overline{\text{PBOE}}$) internal S-space writes will be enabled through to them.
- During DMA I/O $\overline{\text{PBOE}}$ behaves in exactly the same way to the above but by use of the DMAEXT register each of the 4 general purpose DMA channels can be programmed to internal or external space. This means that the behaviour of $\overline{\text{PBOE}}$ during a DMA I/O transfer will depend on whether or not that channel is programmed as external or internal.

Backplane implementation

The motherboard of the Risc PC provides a 132 way edge connector for use with plug in backplane add-ons. Electrically the Risc PC I/O interface supports up to 8 slot backplanes. All decoding needed is provided on the plug-in backplane.

Table 1.5: Risc PC motherboard connector backplane pin-out

Row A	Row B
1 +5V	1 -12V
2 No connection	2 0V
3 $\overline{\text{EASCS}}$	3 LA[27]
4 $\overline{\text{DACK3}}$	4 LA[24]
5 DREQ3	5 LA[25]
6 +5V	6 LA[26]
7 LA[15]	7 0V
8 LA[14]	8 LNBW
9 LA[23]	9 $\overline{\text{MSEL}}$
10 +5V	10 0V
11 LA[13]	11 READY
12 LA[22]	12 $\overline{\text{S7}}$
13 LA[12]	13 0V
14 LA[21]	14 $\overline{\text{S4}}$
15 LA[11]	15 0V
16 LA[20]	16 0V
17 LA[10]	17 $\overline{\text{DACK1}}$
18 LA[19]	18 $\overline{\text{BPPRES}}$
19 No connection	19 0V
20 DREQ2	20 DREQ0
21 LA[9]	21 $\overline{\text{DACK0}}$
22 LA[18]	22 TC
23 $\overline{\text{DACK2}}$	23 $\overline{\text{RST}}$
24 LA[8]	24 0V
25 +5V	25 LRNW
26 LA[17]	26 BD[31]
27 LA[7]	27 $\overline{\text{IOW}}$
28 +5V	28 BD[30]
29 LA[16]	29 $\overline{\text{IOR}}$
30 LA[6]	30 0V
31 LA[1]	31 BD[29]
32 LA[5]	32 0V
33 LA[0]	33 $\overline{\text{PIRQ}}$
34 LA[4]	34 DREQ1
35 LA[3]	35 BD[28]
36 LA[2]	36 $\overline{\text{PBOE}}$
37 BD[15]	37 $\overline{\text{PFIQ}}$
38 BD[14]	38 BD[27]
39 BD[13]	39 BD[26]
40 BD[12]	40 I2CC
41 BD[11]	41 0V
42 +5V	42 $\overline{\text{S6}}$

Table 1.5: Risc PC motherboard connector backplane pin-out

Row A	Row B
43 BD[10]	43 BD[25]
44 +5V	44 I2CD
45 BD[9]	45 0V
46 BD[8]	46 BD[24]
47 BD[7]	47 0V
48 BD[6]	48 BD[23]
49 BD[5]	49 0V
50 BD[4]	50 $\overline{\text{IOGT}}$
51 BD[3]	51 BD[22]
52 CLK2	52 $\overline{\text{IORQ}}$
53 0V	53 BD[21]
54 CLK8	54 0V
55 0V	55 $\overline{\text{BL}}$
56 BD[2]	56 BD[20]
57 BD[1]	57 BD[19]
58 BD[0]	58 BD[18]
59 +5V	59 BD[17]
60 $\overline{\text{SIO}}$	60 BD[16]
61 No connection	61 0V
62 No connection	62 REF8M
63 No connection	63 0V
64 +5V	64 CLK16
65 +5V	65 +12V
66 +5V	66 +12V

Power supply considerations

The power supply fitted inside the Risc PC can be one of two power ratings:

- the basic machine is supplied with a 70W version
- larger machines (e.g. the ACB45) will be equipped with the larger 103W power supply.

The 70W power supply is only designed to be used with a maximum of two fully loaded slots. The larger power supply (103W) has been designed to support up to four fully-loaded backplane slots. The table below outlines the power supply requirement for the Risc PC for the variety of backplane fittings. A power supply capable of supplying the 135W needed for a fully-loaded 8-slot backplane is not available. See the section entitled *Electrical characteristics* on page 1-33 for full power rating breakdown.

Machine	Backplane	Power Supply (power) Requirement
Risc PC	None	70W
Risc PC	2 slot	70W
Risc PC	4 slot	103W
Risc PC	8 slot	135W

Risc PC available add-ons

To contain large backplanes the Risc PC needs to be taller; this is done by adding slices to the middle sections of the case. The following table details the middle section pieces needed to support each of the backplanes.

Machine	Backplane	No of middle sections needed (including original)
Risc PC	None	1
Risc PC	2 slot	1
Risc PC	4 slot	2
Risc PC	6 slot	3
Risc PC	8 slot	4

Description of backplane signals

Table 1.6 shows the pin-out of a standard Enhanced Expansion bus slot. This pin-out relates to expansion slots 0 and 1 only. Expansion slots 2 to 7 are identical with the exception of the DMA control signals.There are no DMA signals on expansion slots 2 to 7 and the relevant pins are No-Connects. The new pin-out is fully compatible for use with existing hardware fitted with the old 64 way (row a and c) connector. Following the table there are functional descriptions of the signals.

Table 1.6: Acorn enhanced expansion bus pin-out

Pin	A	B	C
1	0v	0v	0v
2	LA[15]	nBW	-5v
3	LA[14]	LA[23]	0v
4	LA[13]	LA[22]	0v
5	LA[12]	LA[21]	Ready
6	LA[11]	LA[20]	$\overline{MS}$
7	LA[10]	LA[19]	DRQ[1]
8	LA[9]	LA[18]	DACK[1]
9	LA[8]	LA[17]	Reserved
10	LA[7]	LA[16]	Reserved
11	LA[6]	LA[1]	TC[1]
12	LA[5]	LA[0]	$\overline{RST}$
13	LA[4]	0v	PR/$\overline{W}$
14	LA[3]	BD[31]	$\overline{IOWR}$
15	LA[2]	BD[30]	$\overline{IORD}$
16	BD[15]	BD[29]	$\overline{PIRQ}$
17	BD[14]	BD[28]	$\overline{PFIQ}$
18	BD[13]	BD[27]	EAS
19	BD[12]	BD[26]	I2Cclk
20	BD[11]	BD[25]	I2Cdat
21	BD[10]	BD[24]	Reserved
22	BD[9]	0v	$\overline{PS}$
23	BD[8]	BD[23]	$\overline{IOGT}$
24	BD[7]	BD[22]	$\overline{IORQ}$
25	BD[6]	BD[21]	$\overline{BL}$
26	BD[5]	BD[20]	0v
27	BD[4]	BD[19]	CLK2

Table 1.6: Acorn enhanced expansion bus pin-out

Pin	A	B	C
28	BD[3]	BD[18]	CLK8
29	BD[2]	BD[17]	REF8M
30	BD[1]	BD[16]	+5v
31	BD[0]	0v	CLK16
32	+5v	+5v	+12v

1. The Risc PC only supports DMA on slots 0 and 1 of the backplane

Name	Type	Function	Active
LA[0..23]	O	Latched version of the main system address bus	
BD[0..31]	I/O	Buffered version of main system data bus[1].	
nBW	O	When low indicates byte wide access, when high indicates word or half-word access. Not used during DMA transfers.	
Ready	I	Used to stretch extended address space access cycles	L
$\overline{MS}$	O	Module select. Select signal for module space. Requires control of IOGT signal.	L
DRQ	I	DMA request.	H
$\overline{DACK}$	O	DMA acknowledge.	L
TC	O	Terminal Count. Indicates last cycle of DMA transfer is taking place.	H
$\overline{RST}$	I/O	Reset. Indicates system reset.	L
PR/$\overline{W}$	O	When high this signal indicates that the cycle taking place is a read cycle, when low it indicates that it is a write cycle.	
$\overline{IOWR}$	O	Write strobe for I/O space access cycles.	L
$\overline{IORD}$	O	Read strobe for I/O space access cycles.	L
$\overline{PIRQ}$	I	Interrupt request. Must be open-collector drive.	L
$\overline{PFIQ}$	I	Fast interrupt request. Must be open-collector drive.	L
$\overline{EAS}$	O	Extended address space select signal	L
I2Cclk	I/O	System I²C bus clock signal.	
I2Cdat	I/O	System I²C bus data signal.	
Reserved		Reserved for future use.	
$\overline{PS}$	O	Podule select. Select signal for Podule address space.	L
$\overline{IOGT}$	I	I/O Grant. Used to terminate Module address space access.	L
$\overline{IORQ}$	O	I/O Request. Qualifies MS signal.	L
$\overline{BL}$	I	Buffer latch. Used to control latching of data during Module address space access[1].	L
CLK2	O	2MHz system clock.	
CLK8	O	8MHz system clock.	
REF8M	O	8MHz system reference clock.	
CLK16	O	16MHz system clock.	
+5v		+5 volt supply.	
+12v		+12 volt supply.	
-5v		-5 volt supply.	
0v		System ground.	

1. Only BD[15:0] are valid for data transfers in Podule and Module address space.

Control register definitions

The base address for direct access to the Enhanced Expansion Bus control registers is 0320 0000 hex. The registers are as follows:

Offset	Access	Register	Use
0000	RW	IOCR	Control of I²C bus signals
0020	RO	IRQSTB	Interrupt status
0024	RO	IRQRQB	Interrupt request
0028	RW	IRQMSKB	Interrupt mask
0030	RO	FIQST	Fast interrupt status
0034	RO	FIQRQ	Fast interrupt request
0038	RW	FIQMSK	Fast interrupt mask
00C0	RW	DMATCR	DMA cycle timing control
00C8	RW	ECTCR	Expansion card timing control register
0100	RW	IO0CURA	DMA channel 0, current pointer for block A
0104	RW	IO0ENDA	DMA channel 0, end pointer for block A
0108	RW	IO0CURB	DMA channel 0, current pointer for block B
010C	RW	IO0ENDB	DMA channel 0, end pointer for block B
0110	RW	IO0CR	Control register for DMA channel 0
0114	RO	IO0ST	Status register for DMA channel 0
0120-0134			Registers for DMA channel 1
0140-0154			Registers for DMA channel 2
0160-0174			Registers for DMA channel 3
01F0	RO	DMAST	DMA interrupt status
01F4	RO	DMARQ	DMA interrupt request
01F8	RW	DMAMSK	DMA interrupt mask

Bit definitions

Only those bits relevant to the expansion bus are defined. Other bits will have other functions and must be preserved. In normal use direct access to these registers should be avoided. All access should be via software interfaces defined in the *RISC OS 3 Programmer's Reference Manual*.

Register: IOCR

Reset state: &FF

Bit position	Description
1	I²C clock
0	I²C data

Register: IRQSTB

Reset state: (RO)

Bit position	Description	
5	PIRQ	A 1 indicates that an expansion bus interrupt is pending.
0	PFIQ	A 1 indicates that an expansion bus FIQ is pending.

Register: IRQRQB

Reset state: (RO)

Bit position	Description
5	IRQSTB[5] & IRQMSKB[5]
0	IRQSTB[0] & IRQMSKB[0]

This register represents the logical AND of IRQSTB and IRQMSKB.

Register: IRQMSKB

Reset state: &00

Bit position	Description	
5	PIRQ	A 1 written to this bit enables expansion bus interrupts.
0	PFIQ	A 1 written to this bit enables expansion bus FIQs as regular speed interrupts.

Register: FIQST

Reset state: (RO)

Bit position	Description	
6	PFIQ	A 1 indicates that a fast expansion bus interrupt is pending.

Register: FIQRQ

Reset state: (RO)

Bit position	Description
6	FIQSTB[6] & FIQMSKB[6]

This register represents the logical AND of IRQSTB and IRQMSKB.

Register: FIQMSK

Reset state: &00

Bit position	Description	
6	PFIQ	A 1 written to this bit enables fast expansion bus interrupts.

Register: DMATCR

Reset state: Undefined

Bit position	Description
7 & 6	Control for timing of DMA channel 3
5 & 4	Control for timing of DMA channel 2
3 & 2	Control for timing of DMA channel 1
1 & 0	Control for timing of DMA channel 0

For each pair of timing control bits the DMA access cycle type allocation is:

00 – Type A, 01 – Type B, 10 – Type C, 11 – Type D

Register: ECTCR

Reset state: Undefined

Bits 7 through 0 control the extended address space access cycle type for the eight possible expansion slots.

In each case the cycle type allocation is:

0 – Type A, 1 – Type C

DMA Control registers

A full explanation of the use of the DMA control registers is beyond the scope of this document. Please refer to the *RISC OS 3 Programmer's Reference Manual* for further details of the DMA channel control registers and DMA data transfers. Additional information may be found in the document *DMA Software Functional Specification.*

I/O memory map

The I/O space is split into three, with the upper area (0800 0000 onwards) allocated to EASI and the other two areas are used for podule and module space. The position of podule and module I/O space on the Risc PC is identical as on previous Acorn platforms. In addition, four extra slots (4 to 7) are supported for podule and module space on the Risc PC. The Risc PC I/O physical memory map is shown in *Figure 1.22* on page 1-25.

Signal timings

The following four diagrams show how each of the I/O cycle types included in the DEBI specification occur and upon which clock edges they are timed. All four cycle types shown (A, B, C and D) are supported for DMA transfers, and just types A and C are used as part of EASI. They are intended to give a functional appreciation of the subsequent timing diagrams which detail the exact temporal relationships.

Table 1.7: I/O and DMA I/O bus timings

Cycle type	D	C	B	A
Total no ticks (I/O)	4	5	7	9
Total no ticks (DMA)	3	4	7	9
Ncs/Ndack to Niow/r	0.5	0.5	1.5	1.5
Niow/r pulse width	1.0	2.0	3.0	4.0
Niow/r to Ncs/Ndack	0.5	0.5	0.5	1.5
Ncs/Ndack pulse width	2	3	5	7

Figure 1.18: Type D I/O cycle

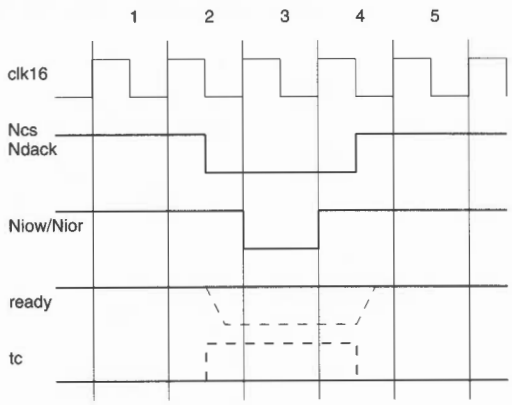


Figure 1.19: Type C I/O cycle

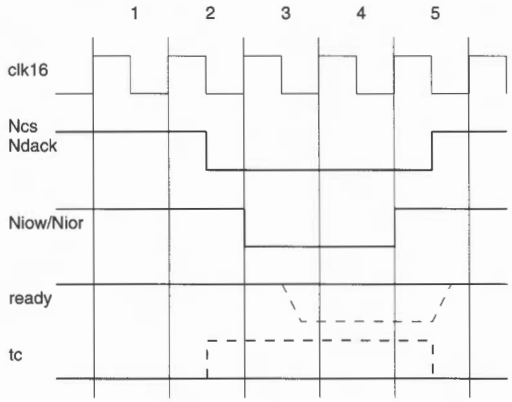


Figure 1.20: Type B I/O cycle

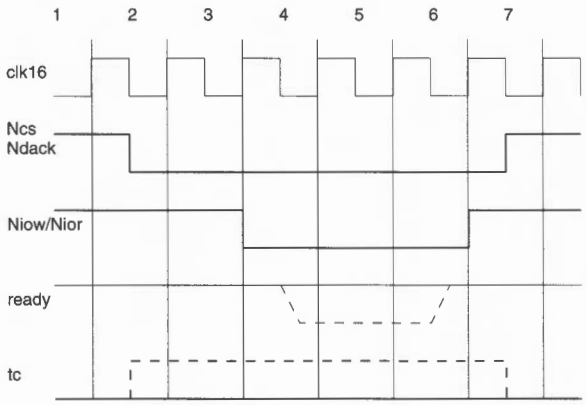


Figure 1.21: Type A I/O cycle

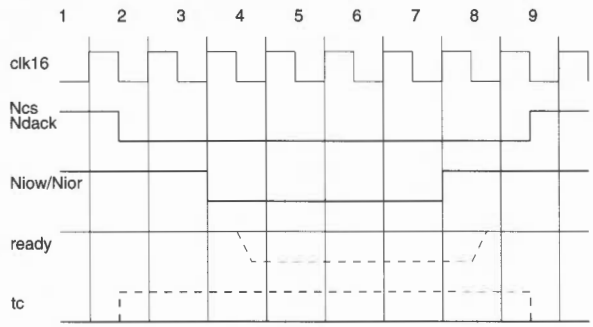


Figure 1.22: Risc PC I/O physical memory map

	&0FFF FFFF
EASI space for expansion card7 (Neasi7)* <16Mbytes 8/16/32 bit width>	&0F00 0000
EASI space for expansion card6 (Neasi6)* <16Mbytes 8/16/32 bit width>	&0E00 0000
EASI space for expansion card5 (Neasi5)* <16Mbytes 8/16/32 bit width>	&0D00 0000
EASI space for expansion card4 (Neasi4)* <16Mbytes 8/16/32 bit width>	&0C00 0000
EASI space for expansion card3 (Neasi3) <16Mbytes 8/16/32 bit width>	&0B00 0000
EASI space for expansion card2 (Neasi2) <16Mbytes 8/16/32 bit width>	&0A00 0000
EASI space for expansion card1 (Neasi1) <16Mbytes 8/16/32 bit width>	&0900 0000
EASI space for expansion card0 (Neasi0) <16Mbytes 8/16/32 bit width>	&0800 0000
Repeat of Podule space with access type 'synchronous'	&033C 0000 to 033F FFFF
Repeat of Podule space with access type 'fast'	&0334 0000 to 0337 FFFF
Repeat of Podule space with access type 'medium'	&032C 0000 to 032F FFFF
	&0327 FFFF
Podule space for expansion card 7 (Nps7 slow)*	&0327 C000
Podule space for expansion card 6 (Nps6 slow)*	&0327 8000
Podule space for expansion card 5 (Nps5 slow)*	&0327 4000
Podule space for expansion card 4 (Nps4 slow)*	&0327 0000
	&0324 FFFF
Podule space for expansion card 3 (Nps3 slow)	&0324 C000
Podule space for expansion card 2 (Nps2 slow)	&0324 8000
Podule space for expansion card 1 (Nps1 slow)	&0324 4000
Podule space for expansion card 0 (Nps0 slow)	&0324 0000
	&0303 FFFF
Module space for expansion card 7 (Nms7)*	&0303 C000
Module space for expansion card 6 (Nms6)*	&0303 8000
Module space for expansion card 5 (Nms5)*	&0303 4000
Module space for expansion card 4 (Nms4)*	&0303 0000
	&0300 FFFF
Module space for expansion card 3 (Nms3)	&0300 C000
Module space for expansion card 2 (Nms2)	&0300 8000
Module space for expansion card 1 (Nms1)	&0300 4000
Module space for expansion card 0 (Nms0)	&0300 0000
	&0000 0000

* Extra address decoding and signal buffering required over and above that provided by the four slot backplane.

Figure 1.23: EASI timings – type A and C

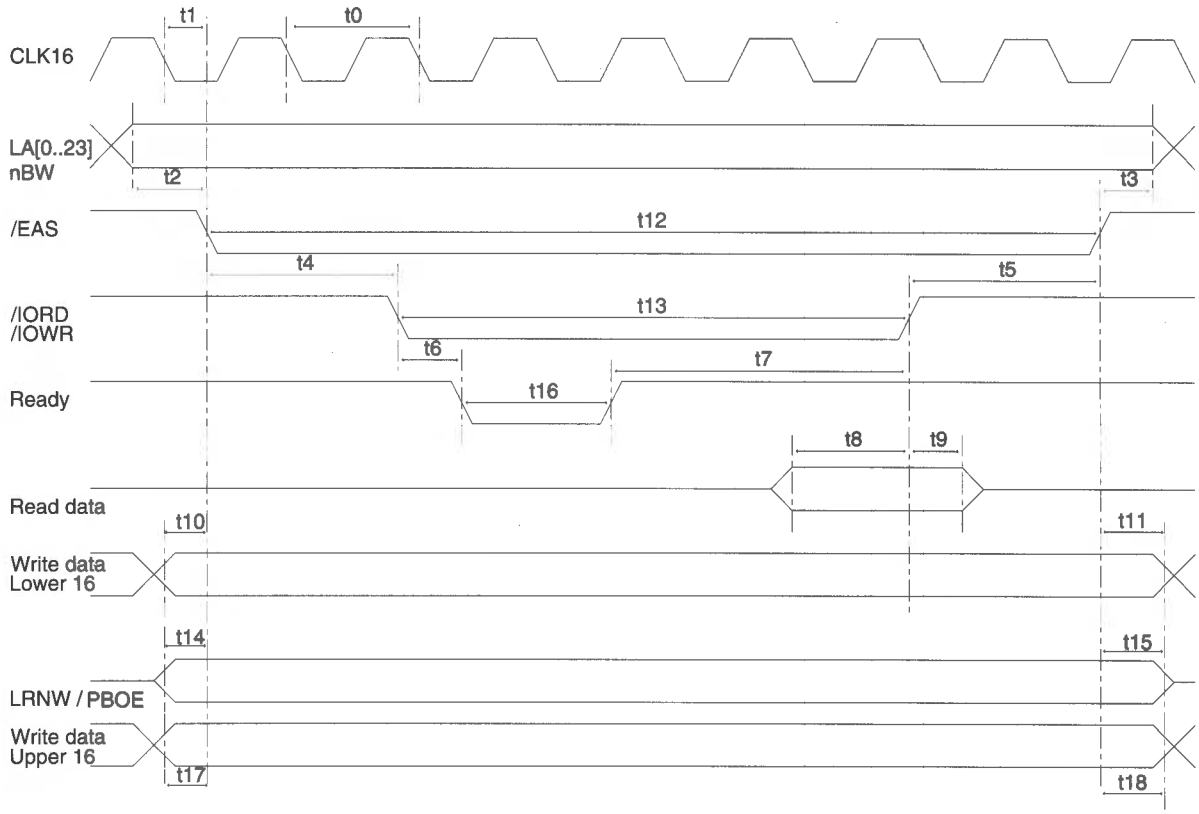


Table 1.8: EASI timings – type A and C

Sym.	Description	Cycles	Min	Typ	Max	Units
t0	CLK16 cycle time	all		62.5		ns
t1	Clock falling edge to $\overline{EAS}$ low	all	5	8	10	ns
t2	Address and nBW setup to $\overline{EAS}$ low	all	270		700	ns
t3	Address and nBW hold from $\overline{EAS}$ high	all	120		1160	ns
t4	$\overline{EAS}$ low to $\overline{IORD}$ or $\overline{IOWR}$	A	90	1.5t0	100	ns
		C	30	0.5t0	40	ns
t5	$\overline{IORD}$ or $\overline{IOWR}$ high to $\overline{EAS}$ high	A	80	1.5t0	100	ns
		C	30	0.5t0	40	ns
t6	$\overline{IORD}$ or $\overline{IOWR}$ low to Ready low	all			50	ns
t7	Ready high to $\overline{IORD}$ or $\overline{IOWR}$ high	A	3t0		4t0	ns
		C	t0		2t0	
t8	Read data setup to $\overline{IORD}$ high (*note 1*)	all	20			ns
t9	Read data hold from $\overline{IORD}$ high (*note 2*)	all	10			ns
t10	Lower 16 Write data setup to $\overline{EAS}$ low	all	150			ns

Table 1.8: EASI timings – type A and C

Sym.	Description	Cycles	Min	Typ	Max	Units
t11	Lower 16 Write data hold from $\overline{EAS}$ high	all	150			ns
t12	$\overline{EAS}$ select width	A		7t0(437)		ns
		C		3t0(185)		ns
t13	$\overline{IORD}$ and $\overline{IOWR}$ strobe width	A		4t0(250)		ns
		C		2t0(125)		ns
t14	LRNW active to $\overline{EASI}$ low	all	150		200	ns
t15	$\overline{EASI}$ high to LRNW in-active	all	130		1300	ns
t16	Ready Strobe width	all	130	max tested 82uS		
t17	Upper 16 Write data Set up to $\overline{EAS}$ low	all	60			ns
t18	Upper 16 Write Data hold from $\overline{EAS}$ high	all	150			ns

Note 1: The lower 16 data bits are strobed into IOMD on the rising edge of CLK16. Internally $\overline{IORD}$ falling and rising edges are synchronous to CLK16. The version of $\overline{IORD}$ seen on the backplane is approximately 10nS lagging the backplane version of CLK16. This effect means that the set-up time quoted on the timing diagram is quoted to take this into account.

Note 2: Due to the effect detailed in *Note1*, the Read data hold time is actually 0 with respect to $\overline{IORD}$ rising edge. Although a hold time of 0 is acceptable for the lower 16 data bits, this value cannot be met by the upper 16 data bits which are latched externally to IOMD and require a hold time of 10nS minimum.

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Figure 1.24: DMA access timings – cycle types A, B, C and D

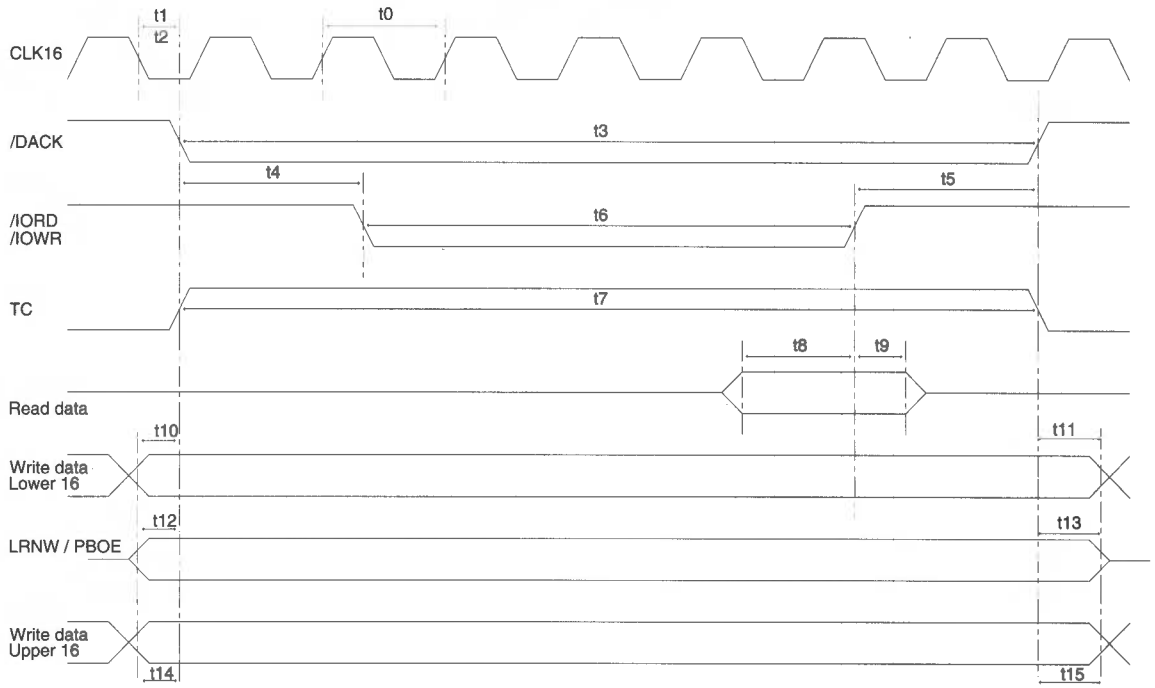


Table 1.9: DMA access timings – cycle types A, B, C and D

Sym.	Description	Cycles	Min	Typ	Max	Units
t0	CLK16 clock cycle	all		62.5		ns
t1	Clock low to $\overline{\text{DACK}}$ low	all	5		10	ns
t2	Clock low to TC high	all	5		10	ns
t3	$\overline{\text{DACK}}$ strobe width	A		7t0(437)		ns
		B		5t0(312)		ns
		C		3t0(185)		ns
		D		2t0(125)		ns
t4	$\overline{\text{DACK}}$ low to $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ low	A, B	80		100	ns
		C, D	30		40	ns
t5	$\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ high to $\overline{\text{DACK}}$ high	A	80		100	ns
		B,C, D	30		40	ns
t6	$\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ strobe width	A		4t0(250)		ns
		B		3t0(185)		ns
		C		2t0(125)		ns
		D		t0(62.5)		ns
t7	TC strobe width	all		t3		ns
t8	Read data setup to $\overline{\text{IORD}}$ high	all	20			ns
t9	Read data hold from $\overline{\text{IORD}}$ high	all	10			ns
t10	Lower 16 Write data setup to $\overline{\text{DACK}}$ low	all	150			ns
t11	Lower 16 Write data hold from $\overline{\text{DACK}}$ high	all	150			ns
t12	LRNW active to $\overline{\text{DACK}}$ low	all	150			ns
t13	LRNW in-active from $\overline{\text{DACK}}$ high	all	130			ns
t14	Upper 16 Write data set up to $\overline{\text{EAS}}$ low	all	60			ns
t15	Upper 16 Hold time from $\overline{\text{EAS}}$ high	all	150			ns

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Figure 1.25: DRQ timings

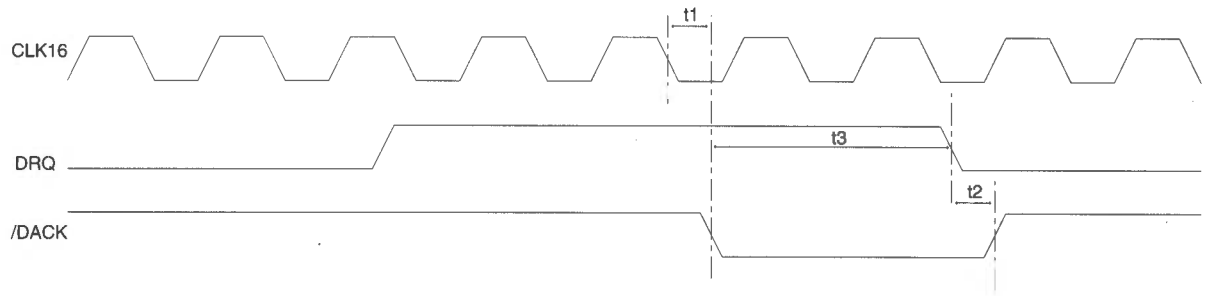


Table 1.10: DRQ timings

Sym.	Description	Min	Typ	Max	Units
t1	$\overline{\text{DACK}}$ low from CLK16 low	0		10	ns
t2	DRQ low to $\overline{\text{DACK}}$ high	15			ns
t3	$\overline{\text{DACK}}$ low to DRQ de-assert	5		see t2	ns

It is allowable to keep DRQ asserted if a peripheral wants to perform multiple DMA cycles. The removal of DRQ at the end of a multiple transfer must still adhere to t2 and t3.

Once asserted, DRQ should never be de-asserted before a responding $\overline{\text{DACK}}$ low as occurred (see t3).

DRQ should only be re-asserted a minimum of 10ns after previous $\overline{\text{DACK}}$ goes high.

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Figure 1.26: Podule address space access timings – cycle types slow, medium and fast

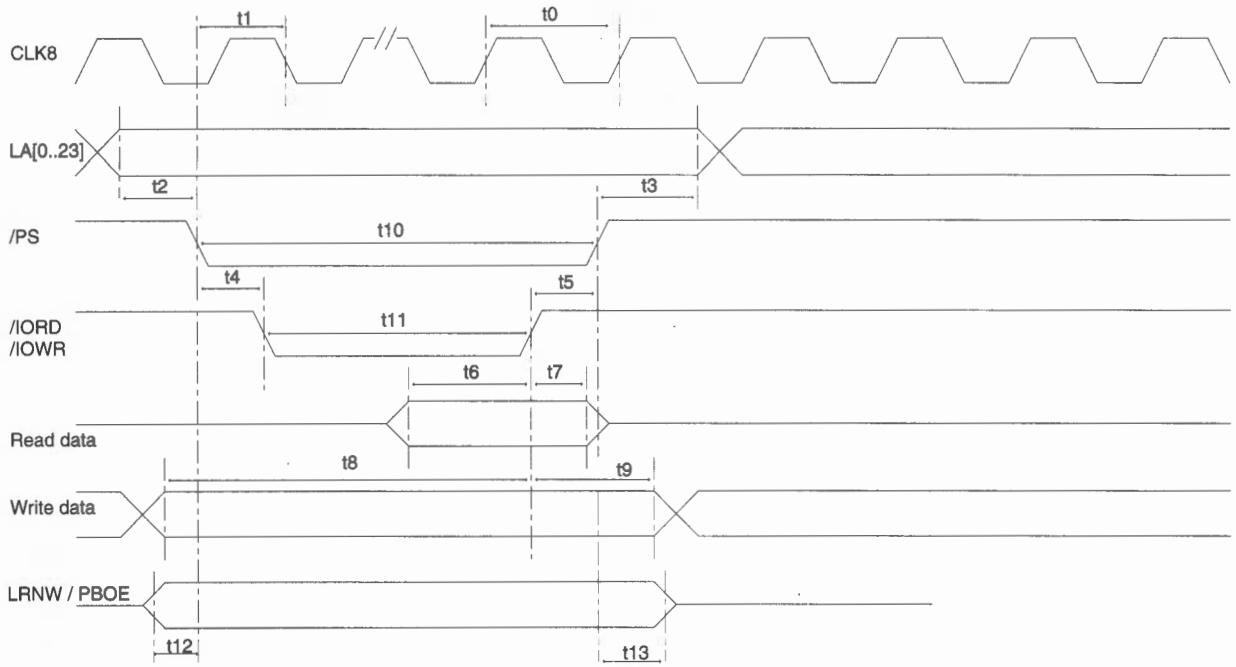


Table 1.11: Podule address space timings – cycle types slow, medium and fast

Sym.	Description	Cycles	Min	Typ	Max	Units
t0	CLK8 pulse width			125		ns
t1	$\overline{PS}$ low to CLK8 low	all	65	77	85	ns
t2	Address setup to $\overline{PS}$ low	all	220		1000	ns
t3	Address hold from $\overline{PS}$ high	all	230	250	800	ns
t4	$\overline{PS}$ low to $\overline{IORD}$ or $\overline{IOWR}$ low	slow	190	210	220	ns
		med/fast	75	85	90	ns
t5	$\overline{IORD}$ or $\overline{IOWR}$ high to $\overline{PS}$ high	slow	100	110	120	ns
		med/fast	105	110	115	ns
t6	Read data setup to $\overline{IORD}$ high	all	15			ns
t7	Read data hold from $\overline{IORD}$ high	all	5			ns
t8	Write data setup to $\overline{IOWR}$ high	all		t4+t11		ns
t9	Write data hold from $\overline{IOWR}$ high	all		t10-t8		ns
t10	$\overline{PS}$ strobe width	slow		$5^1/_2$t0(687)		ns
		medium		$4^1/_2$t0(562)		ns
		fast		$3^1/_2$t0(437)		ns
t11	$\overline{IORD}$ or $\overline{IOWR}$ strobe width	slow		3t0(375)		ns
		medium		3t0(375)		ns
		fast		2t0(250)		ns
t12	LRNW active to $\overline{PS}$ low	all	100		200	ns
t13	$\overline{PS}$ high to LRNW in-active	all	100		1500	ns

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Figure 1.27: Podule address space timings – cycle type synchronous

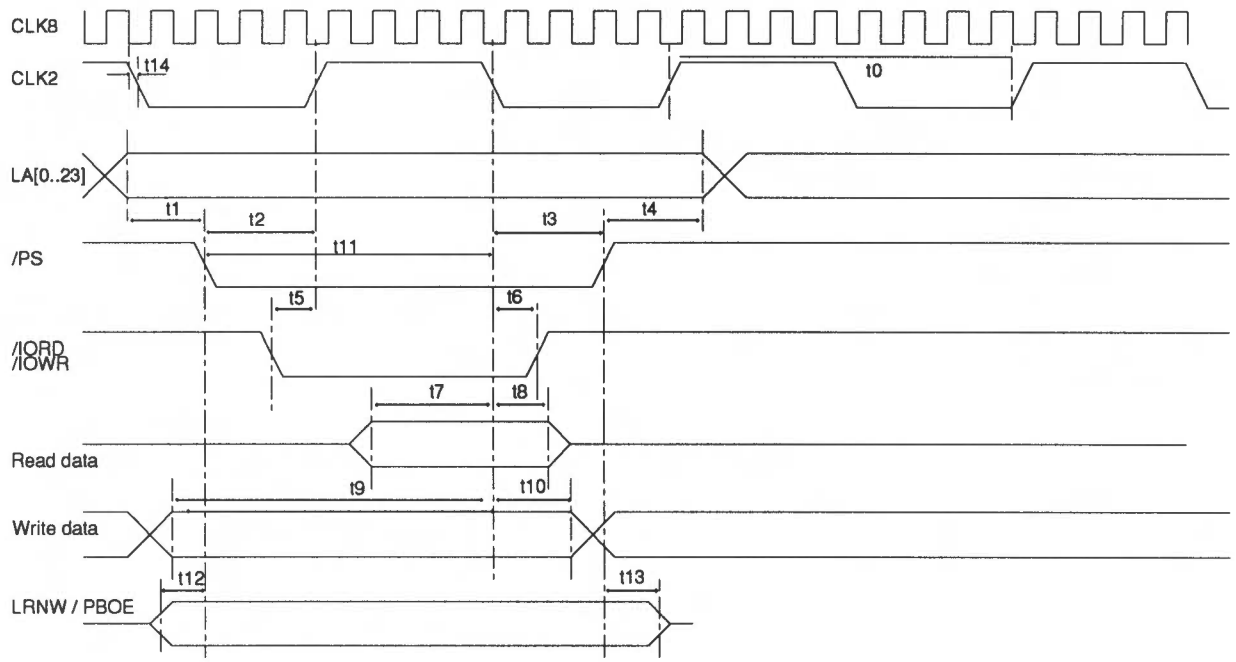


Table 1.12: Podule address space timings – cycle type synchronous

Sym.	Description	Min	Typ	Max	Units
t0	CLK2 clock cycle		500		ns
t1	Address setup to $\overline{PS}$ low	220		1000	ns
t2	$\overline{PS}$ setup to CLK2 high	65	70	80	ns
t3	$\overline{PS}$ hold from CLK2 low	90	100	110	ns
t4	Address hold from $\overline{PS}$ high	230	270	500	ns
t5	$\overline{IORD}$ or $\overline{IOWR}$ setup to CLK2 high	0		10	ns
t6	$\overline{IORD}$ or $\overline{IOWR}$ hold from CLK2 low	0		10	ns
t7	Read data setup to CLK2 falling edge	15			ns
t8	Read data hold from CLK2 falling edge	5			ns
t9	Write data setup to CLK2 falling edge	t11	670		ns
t10	Write data hold from CLK2 falling edge	t11	220		ns
t11	$\overline{PS}$ low to CLK2 low		250		ns
t12	LRNW active to $\overline{PS}$ low	100		600	ns
t13	LRNW in-active from $\overline{PS}$ high	100		1500	ns
t14	CLK8 low to CLK2 low		0		ns

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Figure 1.28: Module address space access timings

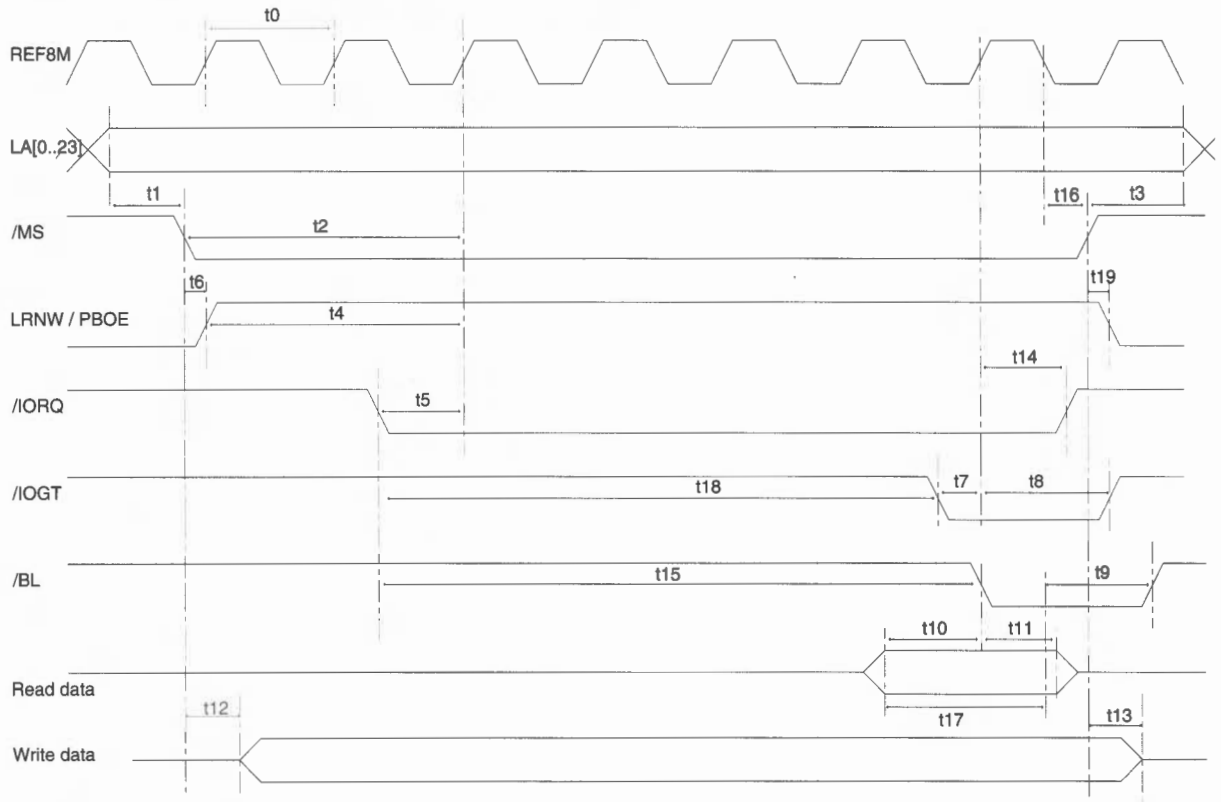


Table 1.13: Module address space access timings

Sym.	Description	Cycle	Min	Typ	Max	Units
t0	REF8M clock cycle time			125		ns
t1	Address setup time to $\overline{MS}$ low		110	120	800	ns
t2	$\overline{MS}$ setup time to REF8M high		120	150	300	ns
t3	Address hold from $\overline{MS}$ high		120		250	ns
t4	LRNW setup to REF8M high		t2			ns
t5	$\overline{IORQ}$ setup to REF8M high		75	85	100	ns
t6	$\overline{MS}$ low to LRNW active			8	12	ns
t7	$\overline{IOGT}$ setup to REF8M high		20		120	ns
t8	$\overline{IOGT}$ hold from REF8M high		0		100	ns
t9	$\overline{BL}$ hold from REF8M low	read	10		100	ns
t10	Read data setup to $\overline{BL}$ low		10			ns
t11	Read data hold from $\overline{BL}$ low		20			ns
t12	Write data setup to $\overline{MS}$ low		8	12		ns
t13	Write data hold from $\overline{MS}$ high			8	12	ns
t14	REF8M high to $\overline{IORQ}$ high			62.5		ns
t15	$\overline{IORQ}$ low to $\overline{BL}$ low		40			ns
t16	$\overline{MS}$ hold from REF8M low		100		1450	ns
t17	Read Data Set up to REF8M low		20			ns
t18	IORQ low to IOGT low[1]				max tested at 82us	
t19	LRNW in-active from $\overline{MS}$ high			8	12	ns

1. IOGT can be delayed from IORQ for an in-definite period of time without effecting the ARM register contents (unlike previous Dynamic ARM processors). The maximum delay tested was as long as 82uS – this figure gave no problems.

Note: These are actual measurements and should not be taken as a specification for the design of interface cards.

Electrical characteristics

Table 1.14: Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Condition
All signals						
Low-level input voltage	V_{IL}			0.8	V	V_{cc}=4.75v
High-level input voltage	V_{IH}	2.0			V	
Low-level output voltage	V_{OL}		0.15	0.26	V	I_{OL} = -4.0mA
High-level output voltage	V_{OH}	3.5			V	I_{OH}=Max V_{cc}=4.75
High-level output current	I_{OH}			-400	uA	V_0 = 3.0v V_{cc}=4.75v
Power available per slot						
Output voltage	V_{cc}	4.75	5.0	5.25	V	
Output current	I_{cc}			1.0	A	
Output voltage	V(+12)	11.4	12.0	12.6	V	
Output current	I_{cc}			250	mA	
Output voltage	V(-5)	-4.75	-5.0	-5.25	V	
Output current	I_{cc}			-10	mA	

Network Interface

The RISC PC is the first Acorn platform to support the new 16 bit network interface. For details of this new standard, refer to *Network Card Mk II Specification* (Part number 0472,208).

The RISC PC supports a DMA channel in addition to the standard set of signals that should be available on a range of future platforms. These are Drq0 on pin B14 and Dack0* on pin C14.There is provision on the motherboard to connect (via two not fitted zero ohm resistors) a second DMA channel (Drq1 on pin C9 and Dack1* on pin B9), but there are no plans to support this second channel as it is reserved for a future motherboard function.

On the RISC PC, the general address decode is done inside IOMD.La<10> & La<11> are used with half an 74ACT139 to provide the final decode for the Net select and NetROM select signals.

&0303 B000 to 0302 B3FF Net select
&0302 B800 to 0302 BBFF Net ROM select

An inverter on the motherboard is used to interface the network card's positive level interrupt to the active low Niext interrupt input into IOMD.

Miscellaneous I/O Decode

IOMD provides the general decode for the motherboard I/O functions. One area of the memory map is known as S space, starting at &0320 0000 which is further decoded by an 74ACT139.

Table 1.15: S space use

Area	Description
S0	is fully decoded inside IOMD, and is used for the IOMD registers.
S1	is used to control reading the mouse buttons, monitor ID and the security link. If the latter is present, the OS prevents the CMOS configuration RAM from being initialised during a 'power up delete'.
S2	Not used
S3	Not used
S4	Tracked to the backplane, where it is further decoded to select podule 0, 1, 2 or 3
S5	Not used
S6	Tracked to the backplane, but not used
S7	Tracked to the backplane, where it can be further decoded to select podule 4, 5, 6 or 7

Part 2 – Interface specifications

Introduction

This chapter provides detailed specifications for each of the interfaces provided on the Risc PC either for future upgrade or for connection of standard peripherals. For each one there is a functional description of the interface, a connector pinout and timing and electrical data. Where applicable the relevant device registers and low level programming interface are outlined; however, this is for information only and is subject to change on future products, even on future revisions of the same product. You should therefore refer to the *RISC OS 3 Programmer's Reference Manual* and the device manufacturers' datasheets listed at the beginning of this manual.

The table below positions each interface within one of three broad areas. This is intended to clarify the use and scope of each interface and, most importantly, highlight those which are likely to remain product-specific. The classifications are:

- **Industry standard**
  unlikely to change significantly in future products. Where applicable non-standard features are highlighted in the text.
- **Acorn proprietary standard**
  Acorn proprietary standard and unlikely to change significantly in future products.
- **Product specific**
  Primarily for internal use only and therefore subject to change; may well be absent on future products.

Table 2.1: Interface classifications

Interface	Classification
Serial	Industry standard
Parallel	Industry standard
Monitor Port	Industry standard
Video Feature and Genlock	Acorn proprietary standard
Audio system	Product specific
Keyboard and Mouse	Industry standard
OPEN Bus	Product specific
DRAM SIMMs	Industry standard
VRAM	Product specific
Floppy Drive	Industry standard
IDE – Hard disc	Industry standard
Network Interface	Acorn proprietary standard
DEBI Interface	Acorn proprietary standard

Keyboard and mouse

Keyboard interface

The keyboard interface is provided by IOMD which contains all the necessary hardware and control registers to provide a fully-functional IBM PC-AT keyboard interface with PS/2 style 6-pin mini-DIN. All signals have EMI filtering.

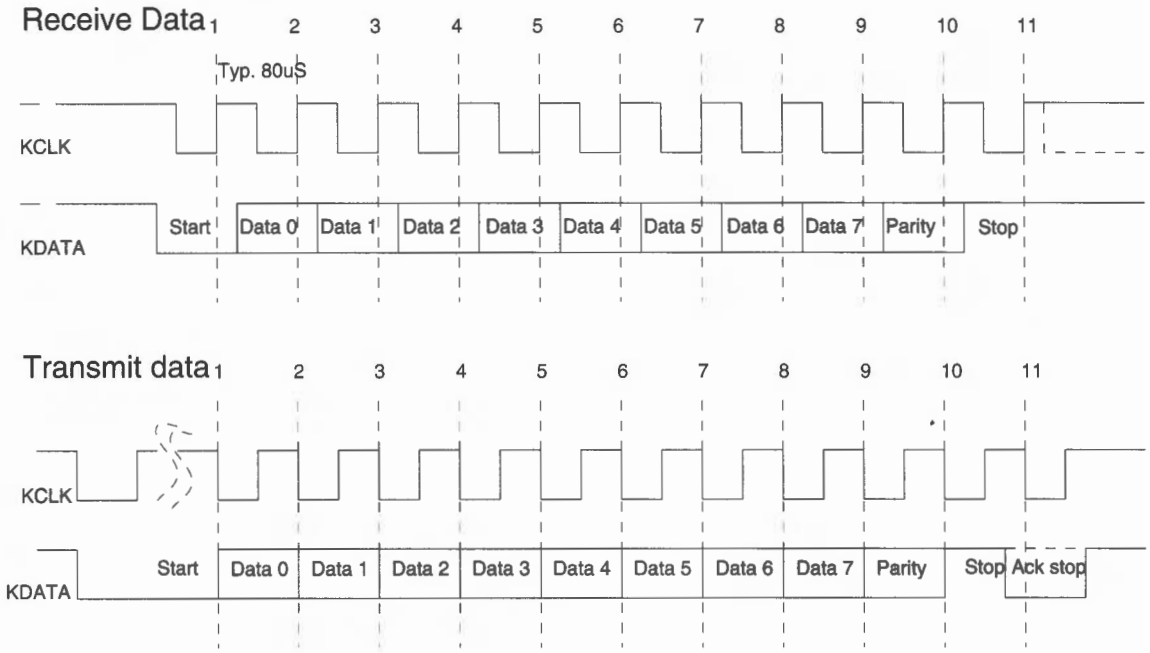
The main features of the interface are

- independent receive and transmit shift registers
- generates processor interrupts on Receive buffer full and Transmit buffer empty
- automatic parity generation for transmit data
- hardware timer for protocol time-out in the event keyboard is unplugged during transmission
- direct drive of keyboard 'Clock' and 'Data' lines.

Data transfer between host system and keyboard micro-controller is via a two-wire synchronous bidirectional serial link. Both signals are open-drain with pull-up resistors. One wire carries the data signal and the other carries the clock signal. The clock signal is always driven by the keyboard device, except when the host system wants to prevent transmission by the keyboard.

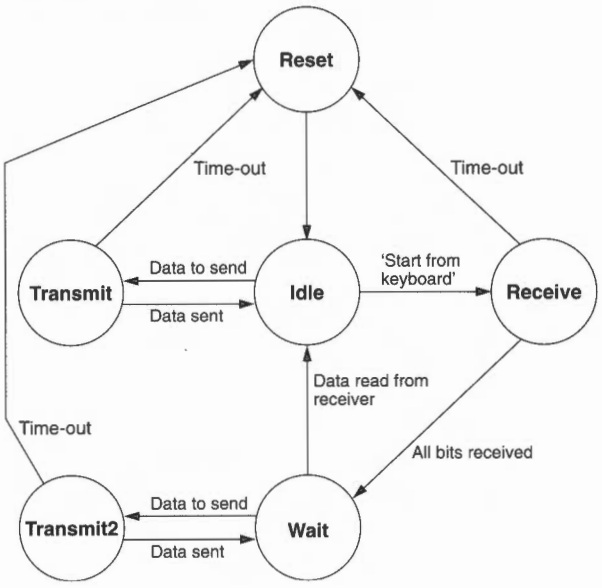
The serial data format is as shown in *Figure 2.1* overleaf.

Figure 2.1: Serial data format



Controller functional description

Figure 2.2: Controller state diagram



A system or power on reset will cause the controller to enter the **Reset** state. It will remain in this state until the Enable bit in the keyboard control register is set.

Once enabled it will move to the **Idle** state, assert the 'transmit register empty' interrupt and remain in this state until one of two possible events occurs:

- If data is written to the transmit register it will go into the **Transmit** state, de-assert 'transmit register empty' interrupt, transmit the data byte in accordance with the IBM PC-AT protocol, and return to the **Idle** state.
- If the clock signal from the keyboard goes low to signal the start of a transmission from the keyboard, the controller moves to the **Receive** state and clocks data from the keyboard into the receive register. When reception is complete the 'Receive register full' interrupt is asserted and the controller moves to the **Wait** state. It remains here until the data received from the keyboard is read out of the receiver register. Further transmission from the keyboard is prevented while in the **Wait** state.

If data is written to the transmit register simultaneously with a start signal from the keyboard then the transmit process has priority and the keyboard is prevented from sending data until transmission to the keyboard is complete. However, if data is written to the transmit register during reception of data from the keyboard, then transmission is delayed until reception is complete.

If data is written to the transmit register while the controller is in the **Wait** state it will move into **Transmit2** state, transmit the data, and then return to the **Wait** state, assuming that the received byte has not been read while transmission was occurring. If it has it will return immediately to the **Idle** state.

If a transmission or reception fails to complete within the time-out period then the state machine will return to the **Idle** state via the **Reset** state.

Start, stop and Ack-stop bits are ignored by IOMD and no framing error checks are made.

Table 2.2: Signal description and connector pinout

Pin	Signal name	Function
1	Kdata	Open drain with 10K pull-up. Data signal synchronised with Kclk passing data between keyboard and host system, and vice versa.
2	NC	Not connected.
3	0V	0v supply.
4	Vcc	5 volt supply filtered and fused at 2A. Maximum permissible current drain 300mA.
5	Kclk	Open drain with 10K pull-up. Clock synchronising data transfer between keyboard and host system, generated by the keyboard.
6	NC	Not connected

Table 2.3: Signal timings

Symbol	Description	Min	Typ	Max	Units
t1	Clock low time	10	40	980	us
t2	Clock high time	10	40	980	us
t3	Clock cycle time	20	80	1000	us
t4	Data hold time from clock high Host system input	2			us
t5	Data set-up time to clock low Host system input	0			us
t6	Data set-up time to clock high Host system output	100			ns
t7	Data hold time from clock low Host system output	0		100	ns
t8	Keyboard inhibited		64		us
t9	Request-to-send grant	1		940	us
t10	Start bit low from request-to-send high			100	ns
	Time-out period		16.336		ms

Figure 2.3: Signal timings

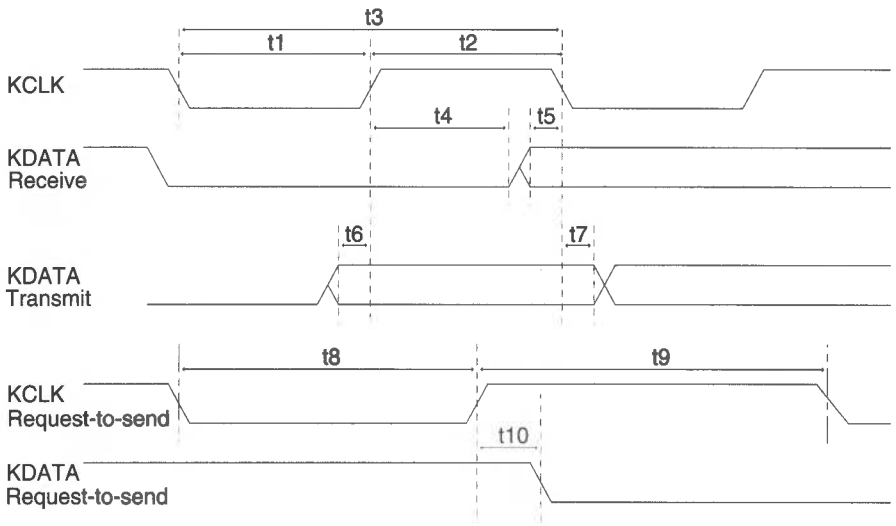


Table 2.4: Electrical characteristics

Parameter		Min	Typ	Max	Units	Test condition
All signals						
Low-level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
High-level input voltage	V_{IH}	2.0			V	
Low-level output voltage	V_{OL}		0.15	0.26	V	I_{OL} = -3.0mA
High-level output voltage	V_{OH}	3.0			V	I_{OH} = max V_{CC} = 4.75V
High-level output current	I_{OH}			100	uA	V_O = 3.0V V_{CC} = 4.75V
Power output						
Output voltage	V_{CC}	4.75	5.0	5.25	V	
Output current	I_{CC}			300	mA	

Control Registers

Direct access to these registers must be avoided.
This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual.*

Table 2.5: IOMD Keyboard control registers

Reg.	Address	7	6	5	4	3	2	1	0
Receive	&0320 0004	Data							
Transmit	&0320 0004	Data							
Status	&0320 0008	TXE	TXB	RXF	RXB	ENABLE	RXPARITY	KDATAI	KCLKI
Control	&0320 0008	R	R	R	R	ENABLE	R	KDATAO	KCLKO
Interrupt									
Status	&0320 0020	KBRX	KBTX	-	-	-	-	-	-
Request	&0320 0024	KBRX	KBTX	-	-	-	-	-	-
Mask	&0320 0028	KBRX	KBTX	-	-	-	-	-	-

Notes

(X=undefined)

Receive (Read only) State following reset = &XX

Data bytes received from the keyboard device are read from this register.

This register should only be read when RXF is true. Reading will clear RXF.

Transmit (Write only) State following reset = &00

Data bytes to be transmitted to the keyboard device are written to this register.

This register should only be written to when TXE is true. Writing will clear TXE.

Status Register (Read only)
State following reset = 00000XXX binary

Bit 7:	TXE	Transmitter empty. Indicates the transmit register is empty and ready to receive data.
Bit 6:	TXB	Transmitter busy. Indicates the transmit is in the process of transmitting data.
Bit 5:	RXF	Receiver full. Indicates that the receiver register contains valid data.
Bit 4:	RXB	Receiver busy. Indicates that the receiver is in the process of receiving data.
Bit 3:	ENABLE	Present state of ENABLE bit in Control register. See below.
Bit 2:	RXPARITY	Parity bit of received data. Always odd parity. Valid only when RXF is set.
Bit 1:	KDATAI	Present state of KDATA signal.
Bit 0:	KCLKI	Present state of KCLK signal.

Control (Write only) State following reset = &00

Bit 7 - 4:	Reserved.	
Bit 3:	ENABLE	When 0 the controller is held in the Reset state. When 1 the controller is allowed to run and KDATAO and KCLKO must be set to 0.
Bit 2:	Reserved.	
Bit 1:	KDATAO	When 1 the external signal KDATA is pulled to 0. When 0 the external signal KDATA is allowed to be pulled to 1.
Bit 0:	KCLKO	When 1 then external signal KCLK is pulled to 0. When 0 the external signal KCLK is allowed to be pulled to 1.

Interrupts

Bits 6 and 7 are used for transmitter-register-empty and receiver-register-full interrupts respectively. Other bits in these registers control other system interrupts and must be preserved at all times.

Interrupt Status (Read only)

Bit 7:	KBRX	When 1 receiver register is full. Cleared by reading receiver register.
Bit 6:	KBTX	When 1 transmitter register is empty. Cleared by writing to the transmitter register.

These flags are identical to RXF and TXE respectively.

Interrupt Request (Read only)

Bits 6 and 7 represent the logical AND of bits 6 and 7 of Interrupt Status and Interrupt Mask registers. Thus a 1 indicates that an interrupt is pending and is not masked, a 0 indicates that either no interrupt is pending or the interrupt is masked or both.

Interrupt Mask (Read/write)

Writing a 1 to the appropriate bit will enable the respective interrupt, writing a 0 will mask the interrupt.

Quadrature Mouse Interface

The Quadrature mouse connector is a standard 9-way mini-DIN socket (Acorn part number 0800,925). The interface is provided by IOMD which contains all the necessary hardware to track mouse movements. The state of the mouse buttons is read from a discrete latch on the Risc PC motherboard. All signals have EMI filtering. A suitable mouse has standard TTL quadrature-encoded outputs (ie. Open-collector outputs providing 0.8mA at 0.4V).

IOMD contains two 16-bit counters, one for X axis movement and one for Y axis movement. For each axis, two signals are produced which are out of phase by 90 degrees and the counters are either incremented or decremented depending on the relative phases of the two signals for that axis. These provide 400 countable events per inch regardless of the speed of the hand (depending on mouse). Alignment and jitter are such that the distance between consecutive pulses is guaranteed. The signals are generated by high precision optical wheels and LEDs.

The four signals are transmitted from the mouse via a ten-wire cable which also carries the status of the three switches, the power supply, an ESD drain, and the power and signal ground.

For further information, you should refer to the IOMD data sheet and the Acorn Medium Resolution 3 Button Mouse Component specification, Acorn part number 0914,001/CS. All software details are covered in the *RISC OS 3 Programmer's Reference Manual.*

Figure 2.4 shows the signals generated for negative and positive movement which increment and decrement the counters respectively on every phase transition.

Figure 2.4: Mouse movement signals

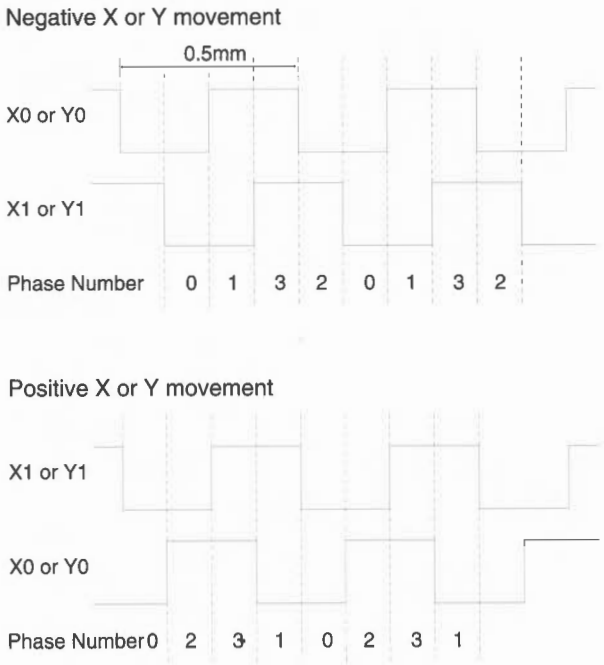


Table 2.6: Signal description and connector pinout

Pin	Signal	Description
1	X1	X axis quadrature signal 1
2	sw1	Left hand side switch: 'Select'
3	sw2	Centre switch: 'Menu'
4	0v	0v supply
5	X0	X axis quadrature signal 0
6	Vsupp	5 volt supply filtered and fused at 2A Maximum permissible current drain 250mA
7	Y1	Y axis quadrature signal 1
8	sw3	Right hand side switch: 'Adjust'
9	Y0	Y axis quadrature signal 0

Figure 2.5: Signal timings

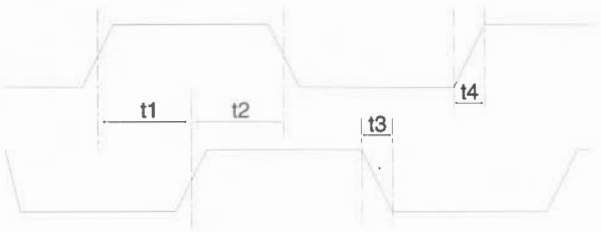


Table 2.7: Signal timings

Symbol	Description	Min	Typ	Max	Units
t1	X1 or Y1 edge to X0 or Y0 edge	5			us
t2	X0 or Y0 edge to X1 or Y1 edge	5			us
t3	Transition time, high to low			100	ns
t4	Transition time, low to high			100	ns

Table 2.8: Electrical characteristics

Parameter		Min	Typ	Max	Units
All inputs:					
Low-level input voltage	V_{IL}			0.8	V
High-level input voltage	V_{IH}	2.0			V
Low-level input current	I_{IL}			-700	uA
High-level input current	I_{IH}			20	uA
Power output:					
Output voltage	V_{CC}	4.75	5.0	5.25	V
Output current	I_{CC}			250	mA

Control Registers

Direct access to these registers must be avoided. This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual*.

Table 2.9: IOMD Mouse control registers

Reg.	Address	Description
MOUSEX	&0320 00A0	16 bit up/down read/write counter
MOUSEY	&0320 00A4	16 bit up/down read/write counter
Following a reset the state of these counters is undefined.		
VID_MSB	&0321 0400	Bit 6 = sw1 Bit 5 = sw2, Bit 4 = sw3 Bit 0 = ID[0]

No de-bounce is provided on the mouse button inputs and this must therefore be achieved in software. Note that the mouse button register is shared with the video monitor ID bit.

Serial port

The interface is provided by an Integrated Input/Output port controller device (often referred to as a 'combo' chip) which contains all the necessary hardware and control registers for the serial port with the exception of processor interrupt control. The interface appears on a 9-way D-type male plug and all inputs and outputs have EMI filtering and voltage level converters.

The Integrated I/O port controller incorporates a full function UART compatible with the industry standard NS16450 and the NS16550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rate is programmable from 115.2K baud down to 50 baud. Character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity. The UART contains a programmable baud rate generator. This first divides the 24MHz reference clock by 13 and then divides this frequency by a number from 1 to 65535. The resulting baud rate is then one-sixteenth of this clock frequency. By altering the contents of the combo chips configuration register, the 24MHz reference clock can be divided by 12 instead of 13, which allows the 31.25 Kbaud data rate of MIDI to be used. However, this is not supported by the operating system. For further details please refer to the FDC37C665, NS16450 and NS16550A data sheets available from Standard Microsystems Corporation and National Semiconductor respectively.

Baud rates supported are:

50	75	110	134.5	150
300	600	1200	1800	2000
2400	3600	4800	7200	9600
19200	38400	56000	115200	

Typical cable capacitance will be 200 pF/m, therefore maximum cable lengths should be as in *Table 2.10*:

Table 2.10: Maximum cable lengths

Data rate (bps)	Cable length (metres)
0 to 20000	10
20000 to 64000	5
64000 to 96000	2
96000 to 115200	1

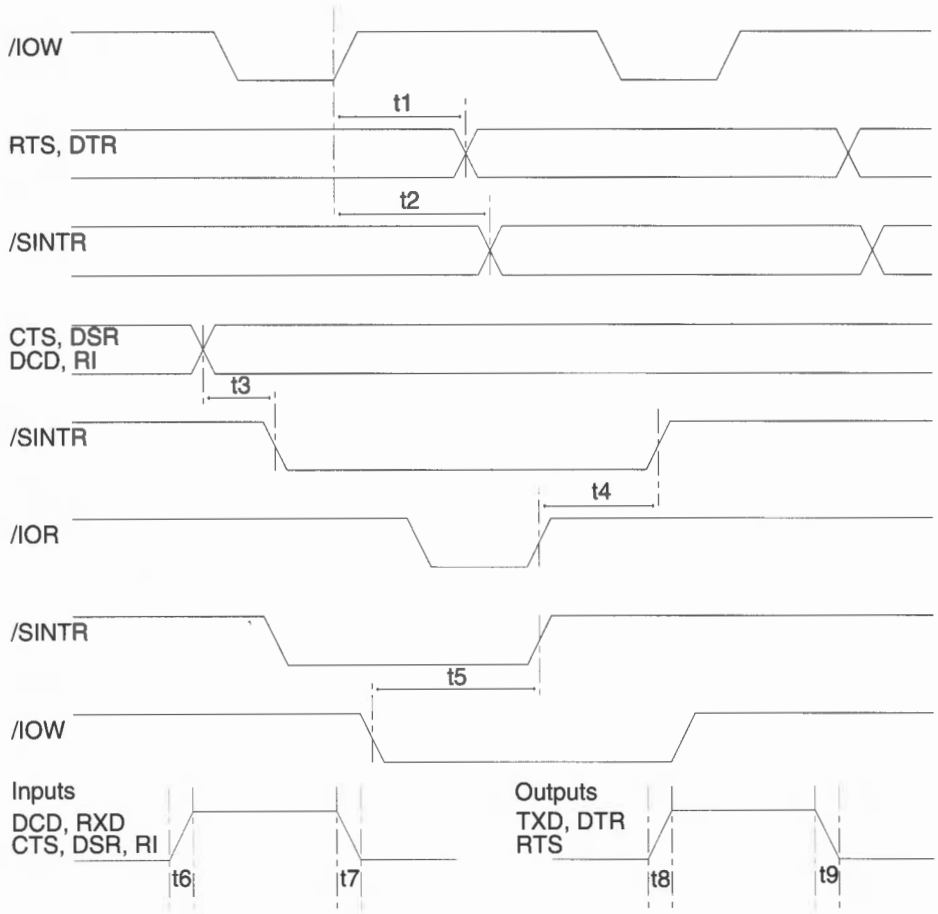
Table 2.11: Connector pinout

Pin	Signal name	Direction	Function
1	DCD	Input	Data Carrier Detect
2	RXD	Input	Receive Data
3	TXD	Output	Transmit Data
4	DTR	Output	Data Terminal Ready
5	0v		Signal ground
6	DSR	Input	Data Set Ready
7	RTS	Output	Request To Send
8	CTS	Input	Clear To Send
9	RI	Input	Ring Indicator

Table 2.12: Signal timings

Symbol	Description		Min	Typ	Max	Units
t1	/IOW to RTS, DTR delay (z = 3.0k and 15pF)	tPLH tPHL			550 375	ns ns
t2	/IOW to /SINTR tri-state delay		10		100	ns
t3	/SINTR active delay from CTS, DSR. DCD				200	ns
t4	/SINTR inactive delay from /IOR (trailing edge)				120	ns
t5	/SINTR inactive delay from /IOW (leading edge)				125	ns
t6	/RXD, DCD, CTS, DSR, RI rise time				100	ns
t7	/RXD, DCD, CTS, DSR, RI fall time				75	ns
t8	/TXD, DTR, RTS rise time			55	100	ns
t9	/TXD, DTR, RTS fall time			45	75	ns

Figure 2.6: Signal timings



Control registers

Direct access to these registers must be avoided. This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual*.

Table 2.13: FDC37C665 Serial port control registers

Reg.	Offset	DRAB†	Function	Access
RB	&00	0	Receive Buffer	read
TB	&00	0	Transmit Buffer	write
IER	&04	0	Interrupt Enable Register	read/write
IFR	&08	X	Interrupt Flag Register	read
FCTL	&08	X	FIFO Control	write
BFR	&0C	X	Byte Format Register	read/write
MCR	&10	X	Modem Control Register	read/write
LSR	&14	X	Line Status Register	read/write
MSR	&18	X	Modem Status Register	read/write
SPR	&1C	X	Scratch Pad Register	read/write
DLSB	&00	1	Divisor LSB	read/write
DMSB	&04	1	Divisor MSB	read/write

†DRAB is the Divisor Register Access Bit contained in the Modem Control register. This flag enables access to the serial clock division ratio register. The default base address of the serial port is &0301 0FE0.

Complete definitions for these registers are contained within the NS16450 and NS16550A data sheets.

IOMD Serial port interrupt registers

Table 2.14: Serial port Interrupt registers

Reg.	Address	7	6	5	4	3	2	1	0
Status	&0320 0030	-	-	-	$\overline{\text{Sintr*}}$	-	-	-	-
Request	&0320 0034	-	-	-	$\overline{\text{Sintr*}}$	-	-	-	-
Mask	&0320 0038	-	-	-	$\overline{\text{Sintr*}}$	-	-	-	-

Note: Although the signal Sintr* leaving the FDC37C665 is active low, the bit in the above registers is set to 1 to indicate that Sintr* is active and thus appears above as $\overline{\text{Sintr*}}$ to reflect this inversion.

Interrupt

Bit four is used for all serial port interrupt control.

Other bits in the registers control other system interrupts and must be preserved at all times. Upon power-up or reset the interrupt is masked and cleared.

Interrupt Status (Read only)

A 1 indicates that an interrupt is pending.

A 0 indicates that there is no interrupt.

Interrupt Request (Read only)

A 1 indicates that an interrupt is pending and is not masked.

A 0 indicates that either no interrupt is pending or the interrupt is masked or both. This bit is the logical AND of the Status and Mask bits.

Interrupt Mask (Read/write)

Writing a 1 to this register will enable serial port interrupts.

Writing a 0 will disable serial port interrupts.

Table 2.15: Electrical characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Test Condition
Inputs						
Input current	I_{IL}	-3.6	-8.3		mA	V_{IL} = -25Vdc
		-0.43			mA	V_{IL} = -3.0Vdc
	I_{IH}	3.6		8.3	mA	V_{IH} = +25Vdc
		0.43			mA	V_{IH} = +3.0Vdc
Input Turn-on Threshold Voltage	V_{IH}			2.25	Vdc	
Input Turn-off Threshold Voltage	V_{IL}	0.75			Vdc	
Outputs						
Logic high	V_{OH}	+8.0	+9.0		Vdc	
Logic low	V_{OL}	-8.0	-9.0		Vdc	
Output Short-Circuit Current †						
Positive	I_{OS+}	+6.0	+10	+12	mA	
Negative	I_{OS-}	-6.0	-10	-12	mA	

† Permanent damage may result if all outputs are shorted simultaneously.

Parallel port

The interface is provided by an Integrated Input/Output port controller device (often referred to as a 'Combo' chip) which contains all the necessary hardware and control registers for the parallel port with the exception of processor interrupt control. The interface appears on a 25-way D-type female socket with EMI filtering on inputs and outputs and 4k7 pull up resistors on all control signals. For further details please refer to the FDC37C665 data sheets available from Standard Microsystems Corporation.

The parallel port has three modes of operation:

Table 2.16: Parallel port modes

Mode	Operation
Printer mode	Standard Centronics mode of operation used for printers fitted with Centronics parallel interface connections.
Fast Centronics	Fast Centronics transfer (output only) using the I/O controller's internal FIFO buffer
Bidirectional mode	Used for transferring data from a device such as a scanner or modem. In this mode, the parallel port becomes bidirectional.

Although other modes of operation are supported by the FDC37C665, for example EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port), these are not supported by the operating system and therefore their use is not encouraged.

The default mode of operation for the parallel port is as an IBM PC-AT-compatible Centronics port for use with standard Centronics devices such as printers.

The port may be used for input purposes by making the appropriate operating system calls to change the mode.

In addition a fast Centronics mode is available utilising the $\overline{\text{STROBE}}$ and BUSY signals as hardware handshake signals. This mode requires that the parallel port FIFO is enabled in order to provide the data at the required rate. In this mode the port is capable of transferring data at or near the peak 500Kbytes/sec allowed in the forward direction.

When using screened multi-core cable of typically 200pF/m the maximum permissible cable length for IBM PC-AT compatible Centronics parallel port mode is 2 metres and for Fast Centronics parallel port mode is 1 metre.

Signal description

Table 2.17: Signal description

Signal	Description	Drive Type
$\overline{\text{STROBE}}$	Data strobe Indicates that data on the parallel port is valid or has been read by the system.	ODP
PD0 - PD7	Port data bus Bidirectional bus, configured as output in printer mode and input in bidirectional mode.	O / IO
$\overline{\text{ACK}}$	Acknowledge Indicates that data has been received by the peripheral or that data output by the peripheral is valid.	IP
BUSY	Busy Indicates that the peripheral cannot accept additional data.	IP
PE	Paper end Indicates that the printer is out of paper.	IP
SCLT	Select Indicates that the peripheral is selected.	IP
$\overline{\text{AUTOFD}}$	Automatic feed Causes printer to automatically add one line feed after each printed line.	ODP
$\overline{\text{ERROR}}$	Error Indicates that the peripheral has an error condition.	IP
$\overline{\text{INIT}}$	Initialise Initialises (resets) the peripheral.	ODP
$\overline{\text{SLCTIN}}$	Select input Selects the peripheral.	ODP
0v		Ground

In Printer Mode the 'peripheral' is actually a printer. In Bidirectional Mode, the PE and $\overline{\text{AUTOFD}}$ signals are irrelevant.

Note an overline indicates that a signal is active low.

I = TTL compatible input
O = Output
D = Open drain
P = 4K7 pull-up to V_{CC}

Table 2.18: Connector pinout

Pin	Signal name	Pin	Signal name
1	$\overline{\text{STROBE}}$	2	PD0
3	PD1	4	PD2
5	PD3	6	PD4
7	PD5	8	PD6
9	PD7	10	$\overline{\text{ACK}}$
11	BUSY	12	PE
13	SCLT	14	$\overline{\text{AUTOFD}}$
15	$\overline{\text{ERROR}}$	16	$\overline{\text{INIT}}$
17	$\overline{\text{SLCTIN}}$	18 - 25	0v

Signal timing

Figure 2.7: IBM PC-AT Compatible Centronics Parallel Port Mode Timing

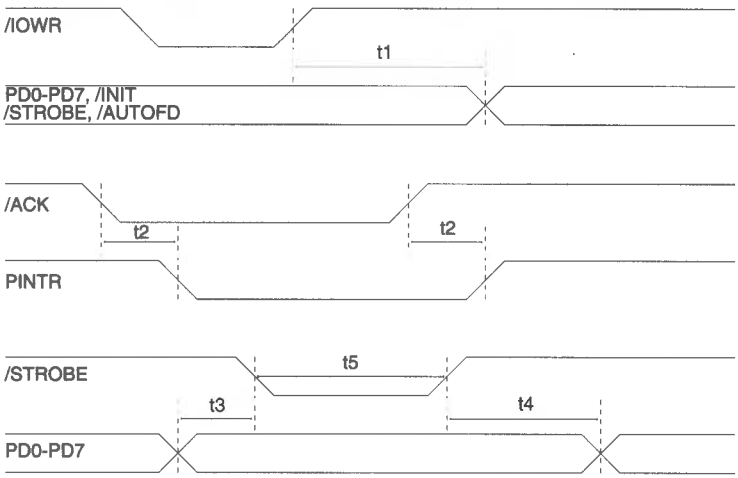


Table 2.19: Centronics mode timing

Symbol	Description	Min	Typ	Max	Units
t1	PD0-PD7, $\overline{\text{INIT}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$, $\overline{\text{SLCTIN}}$ delay from data bus			100	nS
t2	Interrupt delay from $\overline{\text{ACK}}$			60	nS
t3	Parallel data setup time to $\overline{\text{STROBE}}$	1		†	uS
t4	Parallel data hold time from $\overline{\text{STROBE}}$	1		†	uS
t5	Strobe pulse width	1		†	uS

† Time determined by software.

Figure 2.8: Fast Centronics mode parallel port FIFO timing

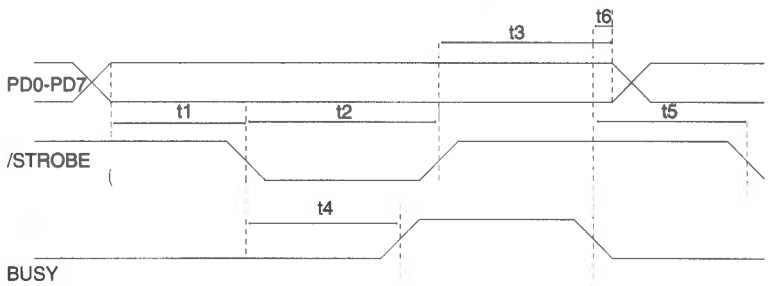


Table 2.20: Fast Centronics mode timing

Symbol	Description	min	max	units
t1	PD0-PD7 valid to $\overline{\text{STROBE}}$ active	600		ns
t2	$\overline{\text{STROBE}}$ active pulse width	600		ns
t3	PD0-PD7 hold from $\overline{\text{STROBE}}$ inactive †	450		ns
t4	$\overline{\text{STROBE}}$ active to BUSY active		500	ns
t5	BUSY inactive to $\overline{\text{STROBE}}$ active	680		ns
t6	BUSY inactive to PD0-PD7 invalid †	80		ns

† The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

Electrical characteristics

Table 2.21: Electrical characteristics

Type	Symbol	Min	Typ	Max	Units	Test Condition
I	I_{IL} I_{IH} V_{IL} V_{IH}	-10 -20 2.0		+10 +20 0.8	uA uA V V	VIN = 0V VIN = V_{CC}
IP	I_{IL} I_{IH} V_{IL} V_{IH}	-0.9 -2.0 2.0		-1.2 +20 0.8	mA uA V V	VIN = 0V VIN = V_{CC}
ODP	V_{OL} V_{OH}	 4.5		0.75	V V	IOL = 10.6mA IOH = -50uA
O	V_{OL} V_{OH}	 2.4		0.75	V V	IOL = 10.6mA IOH = -12mA

Control registers

Direct access to these registers must be avoided. This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual.*

Data Register (Read/write)

Data written to this register is transmitted to the printer. Data read from this port is the data which is on the connector. This port is 100% compatible with the IBM PC-AT parallel port.

Table 2.22: Status register (Read only)

Register	Function	Description
Bit 7	$\overline{\text{BUSY}}$	This bit reflects the state of the BUSY input pin. A 0 means that the printer is busy and cannot accept data. A 1 indicates that the printer is ready to accept data.
Bit 6	$\overline{\text{ACK}}$	This bit reflects the state of the $\overline{\text{ACK}}$ input pin. A 0 means that the printer has received a character and is ready to accept another. A 1 means that it is still reading the last character sent or data has not been received.
Bit 5	PE	This bit reflects the state of the PE input pin. A 1 indicates a paper end condition. A 0 indicates the presence of paper.
Bit 4	SLCT	This bit reflects the state of the SLCT input pin. A 1 means the printer is on-line. A 0 means it is not selected.

Table 2.22: Status register (Read only)

Register	Function	Description
Bit 3	$\overline{\text{ERROR}}$	The bit reflects the inverted state of the $\overline{\text{ERROR}}$ input pin. A 0 means that an error condition has been detected. A 1 indicates no errors.
Bits 2	0	Reserved.

Table 2.23: Control register (read/write)

Register	Function	Description
Bits 7 - 6	Reserved	Reset to 0.
Bit 5	Parallel Control Direction	Valid in extended mode only (controlled by configuration registers). In printer mode the direction is always out regardless of the state of this bit. In bidirectional mode, a logic 0 means that the printer port is in output mode (write), a logic 1 means that the printer port is in input mode (read).
Bit 4	IRQEN	This bit is used to enable or disable interrupts resulting from the printer $\overline{\text{ACK}}$ signal. A 1 generates interrupts when $\overline{\text{ACK}}$ changes from active to inactive. A 0 means that IRQ is disabled. It is recommended that the interrupt control registers in the system core logic be used to enable and disable parallel port interrupts.
Bit 3	SLCTIN	Used to drive the $\overline{\text{SLCTIN}}$ output pin. A 1 selects the printer. A 0 means the printer is not selected.
Bit 2	$\overline{\text{INIT}}$	Used to control the $\overline{\text{INIT}}$ output pin. A 1 allows the printer to run. A 0 initialises the printer.
Bit 1	$\overline{\text{AUTOFD}}$	Used to control the $\overline{\text{AUTOFD}}$ output pin. A 1 causes the printer to generate a line feed after each line printed. A 0 means no autofeed.
Bit 0	$\overline{\text{STROBE}}$	Used to control the $\overline{\text{STROBE}}$ output pin. A 1 in this bit generates the active low pulse (0.5uS pulse minimum) which is required to clock data into the printer. There is a 0.5uS data setup time requirement before $\overline{\text{STROBE}}$ can be asserted. A 0 means there will be no strobe.

Table 2.24: FDC37C665 Parallel port control registers

Reg.	Offset †	7	6	5	4	3	2	1	0
Data	&00	Data							
Status	&04	$\overline{\text{BUSY}}$	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERROR}}$	R	R	R
Control	&08	R	R	DIR	IRQEN	SLCTIN	$\overline{\text{INT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$

† Default base address is &0301 09E0

Table 2.25: IOMD Parallel port interrupt registers

Interrupt	Offset	7	6	5	4	3	2	1	0
Status	&0320 0010	-	-	-	-	-	-	-	PINTR
Request	&0320 0014	-	-	-	-	-	-	-	PINTR
Clear	&0320 0014	-	-	-	-	-	-	-	PINTR
Mask	&0320 0018	-	-	-	-	-	-	-	PINTR

When the parallel port is disabled via the configuration register, all outputs are disabled, and register contents are preserved. Upon power-up or reset, the control signals are inactive. The status register reflects the status signals.

Interrupt

Bit zero is used for all parallel port interrupt control.

Other bits in the registers control other system interrupts and must be preserved at all times. Upon power-up or reset the interrupt is masked and cleared.

Interrupt Status (Read only)

A 1 indicates that an interrupt is pending.

A 0 indicates that there is no interrupt.

Interrupt Request (Read only)

A 1 indicates that an interrupt is pending and is not masked.

A 0 indicates that either no interrupt is pending or the interrupt is masked or both. This bit is the logical AND of the Status and Mask bits.

Interrupt Clear (Write only)

Writing a 1 to this register will clear a pending interrupt.

Interrupt Mask (Read/write)

Writing a 0 to this register will disable parallel port interrupts.

Writing a 1 will enable parallel port interrupts.

Video system

Monitor port

The video connector is a 15-way miniature D-type with a pin allocation very similar to a standard VGA pin-out but with enhancements, as detailed below:

- Pin 9 (normally used for keying) is used to supply +5V, specifically for powering an external UHF modulator or SCART lead.
- Pin 12 provides +12V (source impedance = 1kΩ). This output is used to provide a SCART *function switching* signal for use with SCART TVs.
- Monitor ID sensing on pin 11.

Due to the increased number of screen resolutions, colour depth and monitor options now available, RISC OS 3 Version 3.5 utilises monitor definition files which define individual screen modes in terms of all the relevant timing and control information necessary. The monitor ID scheme previously used on the A5000 is therefore now of limited use and accordingly has been simplified. The ID pin is used by the hardware to recognise the difference between a monitor supporting VGA resolution or better (i.e. with a line rate of 30KHz or more) and a monitor capable of displaying only TV style video such as Mode 12 (i.e. with a line rate of 15KHz). This scheme ensures that a picture is displayed regardless of what monitor is connected to the computer. The ID is only intended to be of use in setting up an initial screen mode, before the mode description file for the user's monitor has been loaded.

Table 2.26: ID Selection

ID[0]	Description	Monitor type	Screen Mode	Sync Type
0	VGA capable	3	27	0
HSync	TV standard	0	12	1
1	Not defined	(as above in RISC OS 3 Version 3.5)		

Some monitors support Display Power Management Signalling or DPMS. This allows a monitor to be placed in a power saving stand-by mode by turning off the HSync, Vsync signals or both. The Risc PC supports this newly created VESA standard; for more details refer to the *RISC OS 3 Programmer's Reference Manual.*

Table 2.27: 15 Pinout of high density D socket

Pin	Signal	Comments
1	Red	
2	Green	
3	Blue	
4	n/c	
5	Gnd	
6	Gnd	
7	Gnd	
8	Gnd	

Table 2.27: 15 Pinout of high density D socket

Pin	Signal	Comments
9	+5v	Proprietary (normally keying)
10	Gnd	
11	ID[0]	
12	+12v	Proprietary (normally n/c)
13	H / C Sync	Composite sync option is Proprietary
14	V / C Sync	Composite sync option is Proprietary
15	n/c	

Signal specification

- RGB
  Source impedance: 75 ohms
  Signal level: 0 to 0.7v positive into 75 ohms
- Horizontal/Comp Sync & Vertical/Comp Sync
  Source impedance: 75 ohms
  Signal level: 5v typ into open circuit
  (Exceeds minimum TTL thresholds into 1K)
- ID[0] 4K7 pull-up to +5v
  High - above 2.0v
  Low - below 0.8v
- +5v feed for TV modulator (SCART control via external series resistor)
  Maximum specified current rating: 75mA
- +12v (feed for SCART function switch control)
  Source impedance: 1K
  Voltage output: 11.25v typ into open circuit

Video Feature Connector

The Video Feature Connector provides an 8-bit control port for use with video overlay, along with horizontal and vertical sync signals and a genlock interface on a 2-row by 8-way 2mm pitch header. The pinout and signal set differs from older Acorn platforms such as the A5000 in order to accommodate the advanced VIDC20 functionality.

Genlock is provided in the same manner as on the A5000. The input **Sink** is provided which resets VIDC's vertical counter to the first raster. Horizontal locking is achieved using an external VCO and phase comparator to generate **Hclk** so as to keep **Hsync** in phase with the external video source Hsync signal.

An 8-bit control port ED[7:0], is provided which allows analogue video mixing or fading to be implemented on a pixel-by-pixel basis. This is the External Data output port from VIDC20 and may be switched to come from either

- one of the R, G or B Look Up Tables (LUT), thus providing a digital equivalent of the analog video output
- or directly from a concatenation of VIDC's 'External register' and external LUT.

This may be used for a variety of purposes such as fading, supremacy, or serialisation for driving very high resolution monitors.

VIDC's external control register EREG[31:0] controls among other things, the nature of the data output on ED[7:0]. For normal operation, RISC OS sets EREG[14:12] to the binary value 001 which configures VIDC to disable Hi-res (bit serialisation), LCD and DAC power-down modes. *Table 2.28* shows the resulting data that appears on ED[7:0] under control of EREG[1:0]. ED[7:0] should be sampled on rising edges of Eclk and EREG[2] must be set to 1 to enable Eclk. For further information, refer to the VIDC20 datasheet.

Table 2.28: Data output on ED[7:0]

EREG[1:0]	ED[7:0]
00	Red LUT[7:0]
01	Green LUT[7:0]
10	Blue LUT[7:0]
11	EREG[7:4], Ext LUT[3:0]

The last entry is the usual configuration for video overlay or supremacy, ED[3:0] is delayed by one pixel so as to coincide with the analogue data to which it corresponds. Because several bits are available, analogue fading and mixing on a pixel-by-pixel basis is possible.

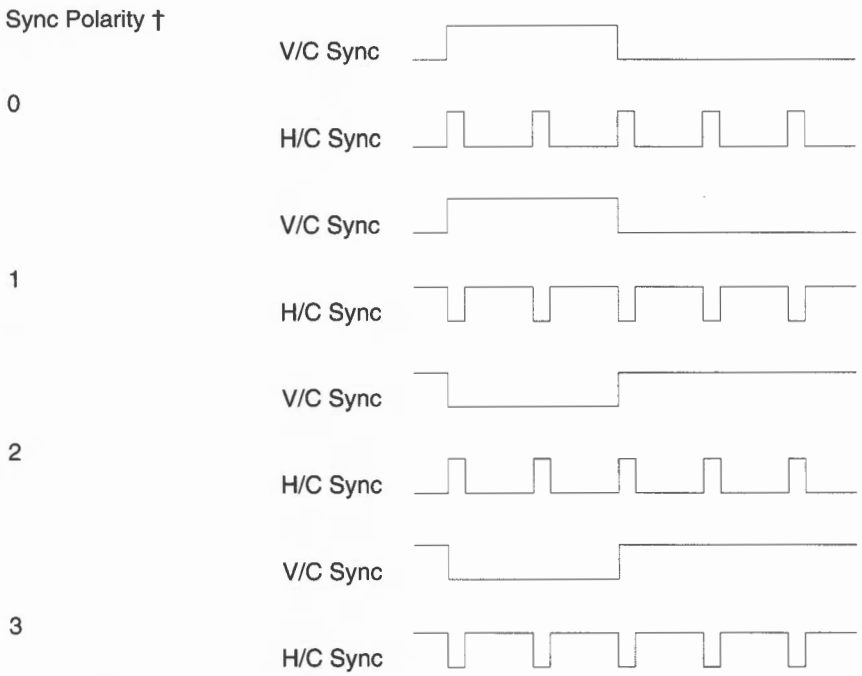
Table 2.29: Signal description

Signal	I/O	Description
H/C Sync	O	Horizontal (or Composite) Sync - same polarity as the monitor port
V/C Sync	O	Vertical (or Composite) Sync - same polarity as the monitor port
Sink	I	High to reset vertical counter. Pulled down with 330R resistor on main PCB
Hclk	I	External clock input for genlock. TTL threshold. Pulled up to +5v with 10 K resistor. VIDC selects between Hclk and VCO clock source under software control.
Eclk	O	VIDC 20 External Data Port clock
Ed[7:0]	O	VIDC 20 External Data Port

Table 2.30: Connector pinout

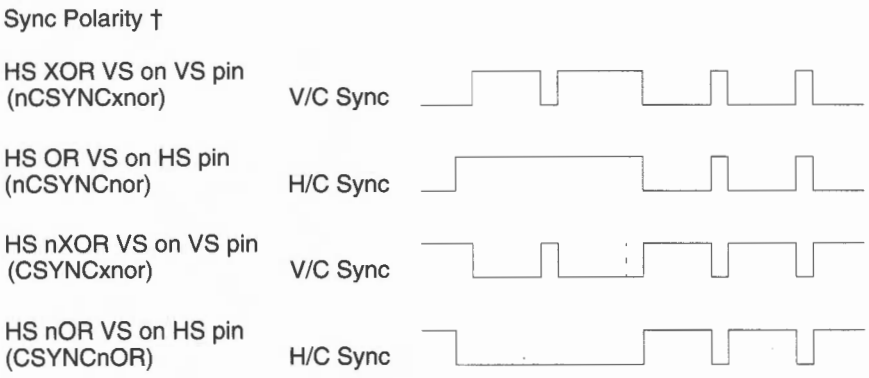
Pin	Signal	Pin	Signal
1	H/C Sync	9	Ed[1]
2	V/C Sync	10	Ed[2]
3	Sink	11	Ed[3]
4	Gnd	12	Ed[4]
5	Hclk	13	Ed[5]
6	Eclk	14	Ed[6]
7	Gnd	15	Ed[7]
8	Ed[0]	16	Gnd

Figure 2.9: Separate sync - (*Configure Sync 0 or *Configure Sync Auto and monitor ID = VGA)



† as defined in the monitor description file

Figure 2.10: Composite sync - (*Configure Sync 1 or *Configure Sync Auto and monitor ID = TV)



† as defined in the monitor description file

Audio system

Auxiliary Audio Connector

The Auxiliary Audio Connector is split between two headers; A and B. Connector A is the same as provided on the A5000 and allows access to the unfiltered left and right sound outputs from VIDC, along with a mono sound input which is mixed in an analogue fashion with the filtered left and right audio signals to produce the internal speaker output.

Connector B is new to the Risc PC and is provided so that the filtered left and right audio channels can be intercepted and an alternative stereo source fed to the stereo sound output jack and internal speaker. It is intended only for use with the 16-bit serial sound upgrade card and may not appear on all future platforms.

Table 2.31: Connector A signal description

Signal	I/O	Description
RawLeft, RawRight	O	Unfiltered Left and Right Audio outputs from VIDC
Left, Right	O	Left and Right Audio outputs after filtering
Aux In	I	Auxiliary mono mixing input for internal speaker

Table 2.32: Connector A pinout

Pin	Signal	Pin	Signal
1	RawLeft	2	0V
3	Left	4	0V
5	Aux In	6	0V
7	Right	8	0V
9	RawRight	10	0V

Table 2.33: Connector B signal description

Signal	I/O	Description
LeftOut, RightOut	O	Left and Right Audio outputs after filtering
LeftIn, RightIn	I	Left and Right Audio Inputs to Headphones and Speaker

Table 2.34: Connector B pinout

Pin	Signal
1	RightIn
2	RightOut
3	LeftIn
4	LeftOut
5	0V (only on 0197,100 PCB)

Serial 16-bit sound interface

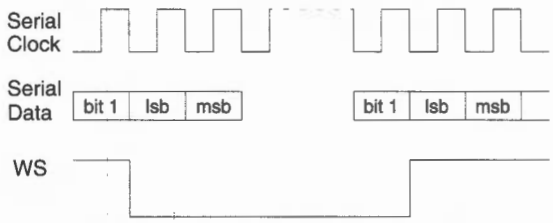
The serial 16 bit sound interface provided on the Risc PC is generated by VIDC20, and for further information you should refer to the VIDC 20 datasheet. The interface is compatible with the Philips I²S standard for interconnecting Audio Compact Disc components, and as such allows a CD digital audio DAC and filter to be connected to VIDC. With the output from the filter applied to the auxiliary audio connector B described previously, a simple but high quality 16-bit sound output is achievable.

VIDC 20 can be configured to use the 16-bit serial interface (digital mode) in preference to the internal VIDC 1 sound core (analogue mode) which is the normal mode of operation.

When in digital mode, bytes from the sound FIFO are output in most-significant order. This is because the serial sound output must go MSB first to be compatible with other serial sound devices. Each byte of data is loaded into a parallel-in, serial-out register, and clocked out under control of the bit clock.

Each 32 bits sample consists of 16 bits for the left hand channel, and 16 bits for the right hand channel. To distinguish between them, a 'word select' (**WS/LnR**) signal is produced. This signal changes when the lsb of the previous word is output. When **WS/LnR** is high, the right hand channel is being output. This timing relationship is shown in *Figure 2.11*.

Figure 2.11: Serial sound output timing



The serial sound output can be used with any DAC with a serial sound input. Many DACs require an 11.2896MHz input clock, in order to derive the 44.1 KHz sample clock. To reduce the number of on board crystals required, VIDC20 can cope with this frequency on the **SCLK** input. When using this, the following parameters need to be programmed in the registers.

- Serial sound (SCTL Register bit 2) = 1
- clksel (SCTL Register bit 0) = 1
- Sound Frequency Register = 2

VIDC20 is not limited to operating with this frequency alone, however the Sound Frequency Register must be set to produce the necessary bit rate accordingly.

Table 2.35: Signal description

Signal	I/O	Description
Sclk	I	Sound Clock – Sound system clock input, for provision of asynchronous clock independent of video clock
Ws / LnR	O	Word Select / Left not Right – In digital mode, logic 0 denotes serial data output is for Left channel. In analogue mode, gives same stereo direction information, but polarity is reversed.

Table 2.35: Signal description

Signal	I/O	Description
Sdclk	O	Serial Data Clock – In digital mode, clock is available and validates data on Sdo on rising edges.
Sdo / Mute	O	Serial Data Out / Mute – In digital mode, 16-bit serial sound data is output as alternative 16- bit channels. In analogue mode, signal goes high between samples to allow for DAC settling.

Table 2.36: Connector pinout

Pin	Signal
1	0V
2	Sclk
3	Ws
4	Sdclk
5	Sdo
6	+5V

Stereo Sound CODEC Interface

The system I/O memory controller IOMD used in the Risc PC provides support for a high quality digital audio CODEC such as the Analog Devices' AD1848. Such a device typically allows capture and playback of high quality 16-bit stereo audio samples along with analogue mixing functions, and offers another level of performance over and above the previously-described sound interfaces.

IOMD provides two DMA channels dedicated to the CODEC interface. The playback channel is bi-directional but the capture channel is uni-directional and shared with the VIDC 1A sound system DMA. These are available on a 5-way connector on the Risc PC motherboard; however, the connector is not fitted and there is no direct connection to the IOMD data bus provided. A DEBI card may use these signals to simplify the design of an advanced sound expansion card, but this interface will not be available on future platforms.

Table 2.37: Signal description

Signal	I/O	Description
Scdrq	I	Sound CODEC Capture DMA Request
Spdrq	I	Sound CODEC Playback DMA Request
Scdack*	O	Sound CODEC Capture DMA Acknowledge
Spdack*	O	Sound CODEC Playback DMA Acknowledge
Sndcs*	O	Sound CODEC Chip Select

Table 2.38: Connector pinout

Pin	Signal
1	Sndcs*
2	Spdack*
3	Scdack*
4	Spdrq
5	Scdrq

OPEN Bus

Risc PC is Acorn's first 32 Bit ARM based platform to offer support for more than one CPU bus master. The 'OPEN Bus' interface allows a second processor device to be connected to the system, whilst sharing resources such as memory & I/O with the native CPU. A set of ARM-like data, address and bus control signals is provided for this purpose and these form the OPEN Bus standard. Physical connection is via two 96-way DIN socket connectors on the Risc PC motherboard, of which one must contain the native or host ARM CPU. Not all future platforms will provide two sockets if the host ARM CPU is fitted to the main PCB, and indeed some may not provide any OPEN Bus connection.

OPEN Bus allows two bus masters to co-exist and pass control of the processor bus between each other. They may both access main memory and memory-mapped IO. However, both cards must conform to the OPEN Bus timing specification, which is essentially the same as that of the ARM processor. The operation of the bus is described in this Data Sheet. However, for further information, you should refer to the ARM 610, ARM 700 and IOMD data sheets.

By way of example, OPEN Bus is suitable for interfacing with any of the following:

- another ARM providing a degree of parallel computation
- a second ARM for dedicated tasks such as DSP, network management or graphics pre-processing
- 'foreign' CPUs, such as the Intel 80x86 processor family for support of alternative software products
- true DSP processor for speech I/O or image processing
- application specific devices such as an MPEG video processor.

Because both cards have full access to the machine's resident memory and I/O, OPEN Bus allows a very cost-effective and high-performance system to be implemented with a minimum of hardware overhead.

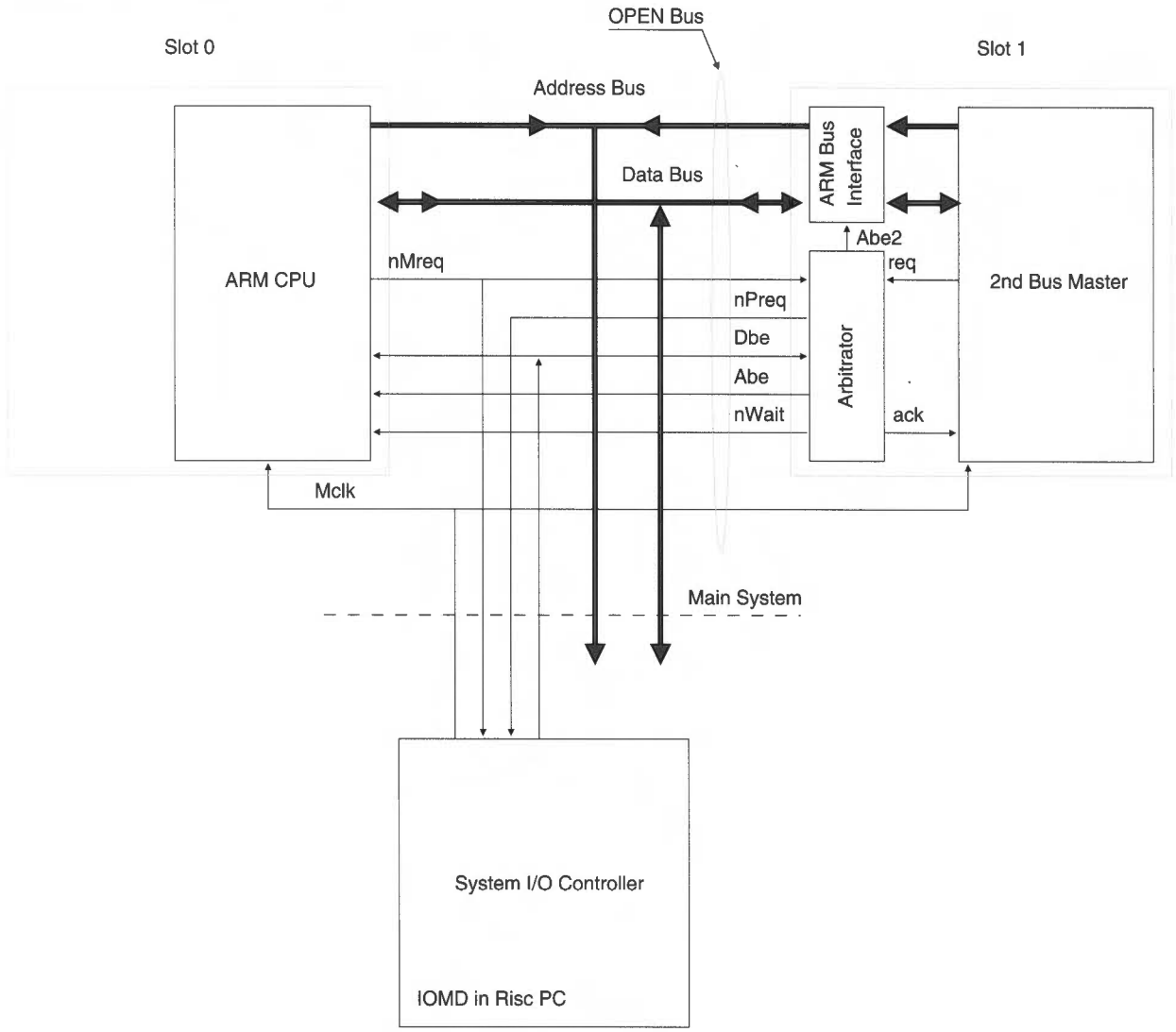
The second OPEN Bus card must contain all the bus arbitration logic to control handing over and claiming of the bus. Host cards only contain the ARM processor itself, clock generation and any co-processing IC that may be appropriate. If the second CPU is not another ARM, there must also be translation circuitry present on the second card to convert the foreign processor's bus protocol to that of the ARM protocol used on the OPEN Bus. Due to the critical timing of some signals and the physical space constraints, the recommended method for implementing such arbitration and conversion circuitry is to make use of an Application Specific IC (ASIC).

Although both Slot 0 and Slot 1 are functionally identical, for consistency and to provide maximum space for second processor cards, the host ARM card should occupy slot 0 and the second card should occupy slot 1.

The Risc PC case gives rise to restrictions on the layout of components on each card as shown in *Figure 2.15* on page 2-22. In most cases, with surface mounted ICs this will not be a problem.

All current Acorn designed host ARM cards only have components on one side of the PCB and can therefore theoretically occupy either slot. However, as stated above it is recommended for consistency that slot 0 is reserved for the host ARM CPU even in a machine with only one card resident.

Figure 2.12: System diagram



Signal description

Table 2.39: Signal description

Name	Function	Main	Host	2nd
A[28:0]	Address Bus. ① Driven by the current bus master.	I	OZ	IOZ
D[31:0]	Data Bus. Driven or read by the current bus master, or tri-stated during DMA operations	IOZ	IOZ	IOZ
MCLK	Memory clock. Driven by IOMD on the motherboard	O	I	I
nR/W	not Read/Write. Driven by the current bus master. Low indicates a read cycle.	I	OZ	IOZ
nB/W	not Byte/Word. Driven by the current bus master. Low indicates to IOMD that only a byte should be written in this cycle.	I	OZ	IOZ
nMREQ	not memory request. Driven low by the host ARM to indicate that it wishes to use the bus in the next cycle.	I	O	I
nPREQ	not processor request. Driven low by the 2nd bus master to indicate to IOMD that it wishes to use the bus in the next cycle. 4K7 pull-up on motherboard.	I	NC	O
DBE	Data bus enable. Driven low by IOMD during DMA. The host ARM and 2nd bus master should both tri-state their data buses when this signal is low.	O	I	I
ABE	ARM bus enable. ② Driven low by the 2nd bus master to tri-state the ARM's address, data and control (nR/W, nB/W and LOCK) buses. 4K7 pull-up on host ARM card.		I	O
nRESET	not reset. System reset line. Main PCB drives this low during power on or other reset.	O	I	I
nFIQ	not fast interrupt request. ③ Provided only on the Risc PC Driven low by IOMD to indicate a fast interrupt request to the host ARM.	O	I	NC
nIRQ	not interrupt request. ③ Provided only on the Risc PC Driven low by IOMD to indicate an interrupt request to the host ARM.	O	I	NC
nWAIT	not wait. ② The 2nd bus master drives nWAIT low to stall the host ARM whilst it is active. 4K7 pull-up on host ARM card.		I	O
LOCK	Locked operation. ② Driven high by the host ARM when executing a SWP instruction to indicate a locked memory cycle.		O	I
nPIRQ	not Podule interrupt. ④ Driven low by the 2nd bus master to interrupt the ARM. Open collector. 4K7 pull-up on motherboard	I	NC	OD

Table 2.39: Signal description

Name	Function	Main	Host	2nd
nPFIQ	not Podule fast interrupt. ④ Driven low by the 2nd CPU to interrupt the ARM. Open collector 4K7 pull-up on motherboard	I	NC	OD
RCLK	Reference clock. ⑤ A less stretched version of MCLK provided by IOMD. Present only on the Risc PC PCB, Untested and missing in future platforms.	O	NC	

All signals are at TTL threshold levels. However, it is recommended that all outputs from the second bus master card should drive to CMOS logic high levels, i.e. >0.7Vcc. This is in order to cater for CMOS input level logic which may be present in future products.

Key

Main Risc PC motherboard

Host Host ARM card

2nd Second bus master

I Input

O Output

Z Signal can be tri-stated

NC For this card, it is expected that this signal will not be connected as it is of no obvious use.

OD Output – Open Drain

① A[29] is tracked between the connectors on the motherboard and is fed into the system address latch, but not used. A second bus master card should not use this signal as it is untested and may be removed.

② ABE, nWAIT and LOCK signals are tracked between the connectors on the motherboard, but are not connected elsewhere on the Risc PC motherboard.

③ The signals nFIQ and nIRQ are provided because on current Risc PC products the native ARM CPU is connected to the system via a 'host' OPEN Bus card. The host ARM must have interrupt access to the system controller IOMD on the motherboard. On platforms where the host ARM processor is fitted to the motherboard and only one OPEN Bus socket is provided solely for a second bus master, these signals will be missing.

④ The use of the podule bus interrupt lines allows easy software integration for second bus master interrupt servicing. An interrupt flag register must be present in the bus interface ASIC to allow the system to identify whether the interrupt was generated by a podule, or the second bus master. An interrupt mask register must also be provided. In addition, a global mask register in IOMD may be used to disable all podule interrupts.

⑤ On current Risc PC products, RCLK is provided as an input to the second bus master card. However, it will not be provided on other platforms, and so a second bus master card must work without this signal.

Table 2.40: OPEN Bus connector pinout

Pin	A	B	C
1	0V	D[0]	D[1]
2	D[2]	D[3]	D[4]
3	D[5]	D[6]	D[7]
4	D[8]	D[9]	0V
5	D[10]	D[11]	D[12]
6	+5V	D[13]	D[14]
7	D[15]	D[16]	D[17]
8	D[18]	0V	D[19]
9	D[20]	D[21]	D[22]
10	D[23]	D[24]	D[25]
11	D[26]	D[27]	D[28]
12	D[29]	D[30]	D[31]
13	DBE	*Tck*	nMREQ
14	0V	*nIRQ*	0V
15	*nFIQ*	nPREQ	*Trst*
16	+5V	nRESET	*Tms*
17	nPFIQ	nPIRQ	*RCLK*
18	ABE	0V	nR/W
19	nB/W	LOCK	*Tdo1*
20	nWAIT	*Tdi*	MCLK
21	A[0]	A[1]	A[2]
22	A[3]	A[4]	A[5]
23	A[6]	A[7]	A[8]
24	A[9]	A[10]	0V
25	A[11]	A[12]	A[13]
26	+5V	A[14]	A[15]
27	A[16]	A[17]	A[18]
28	A[19]	0V	A[20]
29	A[21]	A[22]	A[23]
30	A[24]	A[25]	A[26]
31	A[27]	A[28]	*A[29]*
32	0V	*Tdo2*	0V

Note:

Signals in italics are Risc PC specific and may be absent on future implementations.

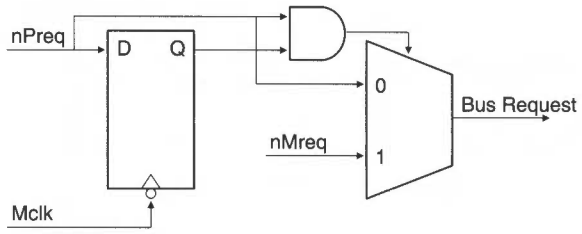
The signals Tck, Trst, Tms, Tdi, Tdo1 & Tdo2 are reserved for boundary scan test signals.

Bus arbitration

Architectural support within the Risc PC for a second bus master is provided by the signal Npreq. Assertion of Npreq instructs the IO/Memory controller IOMD that in the next cycle the second bus master will require the bus. This signal is similar to Nmreq, but with higher priority (see below). The bus conversion circuitry must ensure that un-aligned accesses are converted to ARM byte or word accesses and make sequential accesses truly sequential (thus an 80486 cache line fill, for example, would have to be modified if it did not start on a quad word boundary).

In the following discussions and accompanying diagrams, nMreq, nWait and Abe are the host ARM bus control signals. Additionally, the host ARM processor is referred to as processor 'P1' and the second bus master as processor 'P2'.

Figure 2.13: nPreq / nMreq priority in IOMD



If the arbitrator removes nPreq for only one Mclk period and then reasserts it, IOMD does not relinquish the bus to the ARM and thus P2-Locked cycles (for example) may be performed. If however more than one cycle of nPreq removal occurs, the arbitrator must pass control of the bus back to the host ARM.

Operation

The bus arbitrator must wait for a safe time to commence arbitration, halt P1 using the Nwait signal and remove it from the bus using Abe. It then places P2 on the bus which then performs an access, or burst of sequential accesses. When P2 completes a transfer, or burst of sequential transfers, it removes it's pipelined request, and the arbitrator re-asserts the Abe signal. One cycle later it removes the Nwait signal to the host ARM, which is then free to continue where it left off. This ensures correct internal sequential operation, should the ARM require the bus immediately. The arbitration must be synchronised to Mclk, and arbitrator outputs are nominally driven from the falling edge of Mclk. The ARM Lock signal must also be observed and P2 should not be allowed to request the bus in the internal cycle between the read and write cycles of a Swap instruction.

Cycle Timing

The timing diagram in *Figure 2.14* on page 2-21shows P2 doing a three word burst. This simplified waveform does not show the clock being stretched, which occurs on some cycles to ensure the bus speed is correct for the area of the address space being accessed. The clock is also stretched for other activity such as DMA. To prevent data bus contention in such cases, P2 should stop driving the data bus when the Dbe line is low.

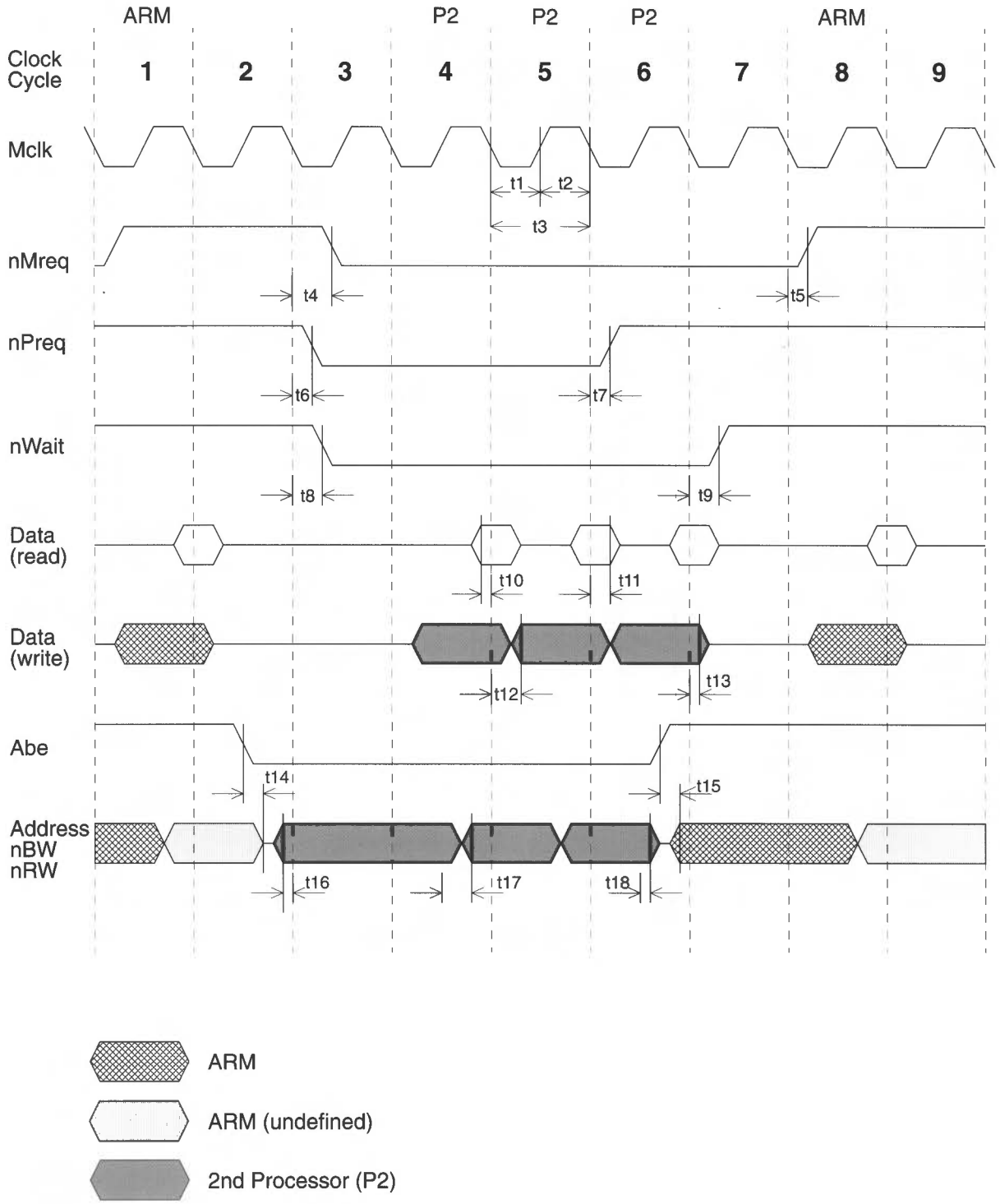
The timing parameters are given in *Table 2.42*. The bus cycles described do not form part of the OPEN Bus specification and a different arbitration scheme may be employed.

The clock cycle activity shown in *Figure 2.14* is described in *Table 2.41*.

Table 2.41: Clock cycle activity

Clock cycle	Activity
1	ARM has the bus. The ARM bus (Abe) remains enabled. The bus arbitrator should check nMREQ is high and Lock is low, and that P2 will require the bus before moving on to cycle #2.
2	Bus change-over. The arbitrator should check nMREQ. If it goes low during this cycle, the ARM will require the bus in the next cycle. Therefore Abe should remain enabled and the bus arbitrator should return to cycle # 1. If nMreq remains high during the Mclk high phase, the address & control bus should be switched, i.e. drive Abe low to disable the ARM bus and then the enable P2 address, & control bus.
3	P2 request cycle. The arbitrator should drive nPreq low to indicate to IOMD that P2 will be using the bus in the next cycle. It should also drive nWait low to stop the ARM needing the bus.
4	P2 has the bus - first cycle
5	P2 has the bus - second cycle
6	P2 has the bus - third cycle As P2 does not require the bus in the next cycle, the nPreq signal should be taken high. During the high phase of Mclk, the address and control bus should be swapped (ie P2 address and control bus should be disabled and Abe enabled)
7	ARM request cycle. nWait should be driven high to allow the ARM to continue where it left off.
8	ARM has the bus
9	Idle bus tick

Figure 2.14: Signal timing and bus cycle



OPEN Bus parameters

Table 2.42: Signal timings for 2nd processor interface

Symbol	Parameter	min (ns)	max (ns)
t1	Mclk low	28	
t2	Mclk high	28	
t3	Mclk period	62	10000
t4	nMreq delay		30
t5	nMreq hold	2	
t6	nPreq delay		20
t7	nPreq hold	2	
t8	nWait delay		23
t9	nWait hold	3	
t10	Read data set-up	2	
t11	Read data hold †	10	
t12	Write data delay		28
t13	Write data hold	3	
t14	ARM bus disable time		15
t15	ARM bus enable time		15
t16	Address & control set-up	5	
t17	Addr & cntrl delay from Mclk rise		23
t18	Addr & cntrl hold from Mclk rise	2	

† t11 depends on the bus capacitance to hold the data, as the memory system does not continue to drive the bus through this period.

Table 2.43: Capacitive loading

Address Bus	max	20	pF
Data Bus I/O	max	20	pF
Control signals	max	20	pF

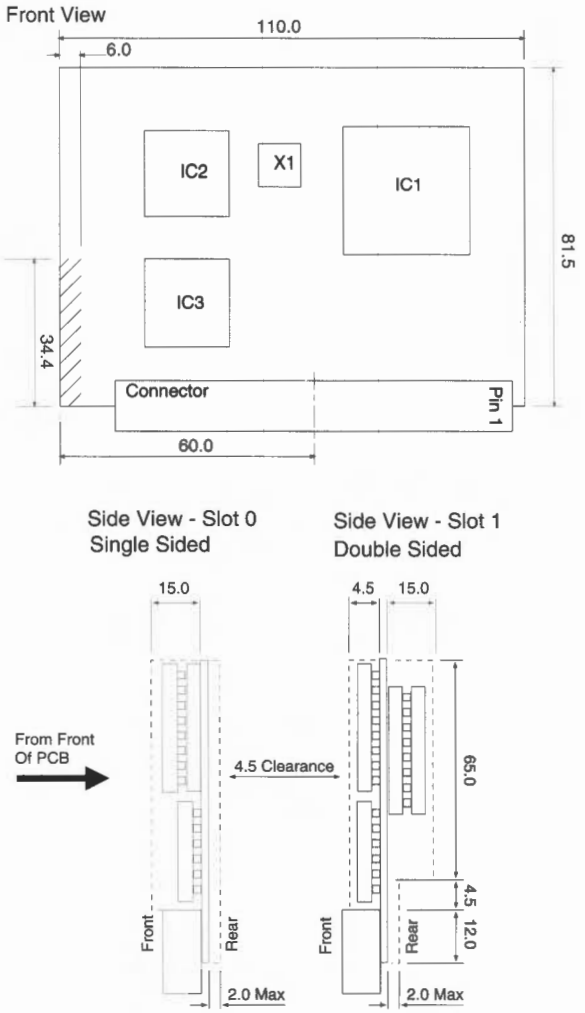
Table 2.44: Drive capability

Address Bus	min	80	pF
Data Bus I/O	min	200	pF
Control signals	min	80	pF

Power consumption allowance

- Host ARM CPU cards should consume no more 500 mA at (5.0 ± 10%) V
- Second bus master cards should consume no more than 1.5A at (5.0 ± 10%) V

Figure 2.15: Physical dimensions and pin orientation



All dimensions in mm
Tolerances: ±0.2 unless specified
The number & orientation of ICs on this diagram is for guidance only.

- No components or copper to encroach into the hatched area on either side of the PCB (to avoid fouling card slot).
- Connector is a standard 96-way right angle DIN 41462 plug.
- Only low power dissipation devices may be fitted on the front of the card in slot 1.
- Board thickness: 1.6mm.

DRAM SIMMs

The Risc PC supports up to 256 MB of DRAM by providing two sockets on the motherboard for industry standard Single In-line Memory Modules or SIMMs. Suitable modules must use square array memory technology, ie. Dynamic RAM devices with the same number of rows and columns. The modules must also support 'Fast Page Mode' and 'CAS before RAS refresh'.

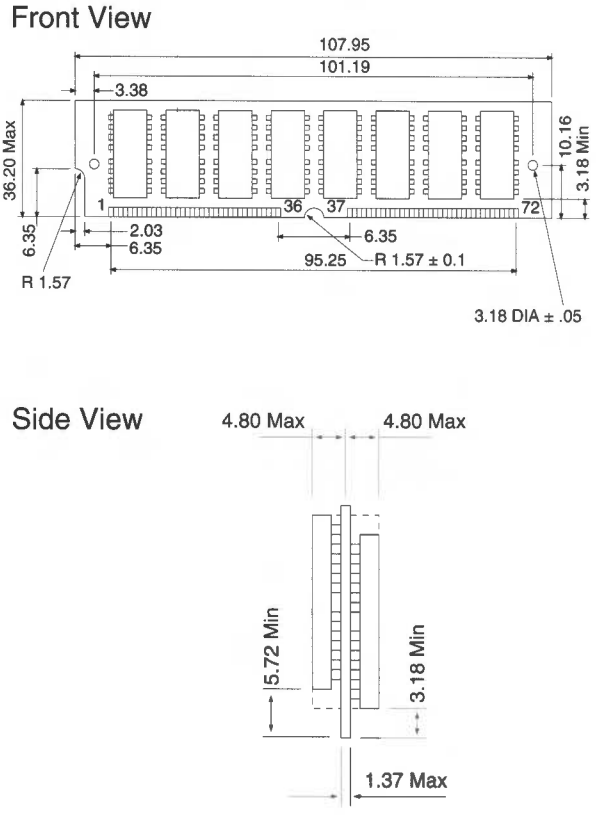
To realise the maximum configuration requires two 128 MB SIMMs. However, at the time of writing, the maximum size of memory SIMM commercially available is 32 MB and to provide more than this requires use of address bit Ra[11]. At present, DRAM suppliers have not yet agreed on which pin should carry this signal. As a result, Ra[11] is connected to pin 29 as this is currently one of the N/C pins as defined by the JEDEC specification and indeed, some suppliers use this pin for Ra[11] on their non-square DRAM arrays. If when larger modules are available Jedec have approved a standard placement for Ra[11] which is not pin 29 it will be necessary to remove the zero ohm resistor in series with RA[11] and reconnect it to the correct N/C pin.

It is possible for larger or application specific SIMMs to be designed using commercially available DRAM ICs. These 'proprietary' modules must meet the dimensional specifications given in *Figure 2.16* closely, in order to mate correctly with the 72 way SIMM connectors. Please note that in this case, it is very likely the increased number of DRAMs will violate the capacitive loading specifications given later on in this document, therefore, it is probable that some form of buffering will need to be implemented on the module itself.

For placement details of DRAM in the Risc PC memory map, you should refer to *Figure 1.7* on page 1-10.

No timing diagrams are given. However, the timing information listed applies to the usual diagrams found in semiconductor vendors' standard databooks.

Figure 2.16: Physical dimensions and pin orientation



Contacts to be tin/lead or gold

All dimensions in mm
Tolerances: ±0.13 unless specified

The number & orientation of ICs on this module is for guidance only.

Table 2.45: Pinout list for both SIMM sockets

Pin No	SIMM Signal	Description	Notes
1	Vss	0v	Connect to Digital ground
2	D[0]		
3	D[16]		
4	D[1]		
5	D[17]		
6	D[2]		

Table 2.45: Pinout list for both SIMM sockets

Pin No	SIMM Signal	Description	Notes
7	D[18]		
8	D[3]		
9	D[19]		
10	Vcc	+5v supply rail	Decoupled & filtered supply
11	N/C		Reserved
12	Ra[0]		
13	Ra[1]		
14	Ra[2]		
15	Ra[3]		
16	Ra[4]		
17	Ra[5]		
18	Ra[6]		
19	Ra[10]		
20	D[4]		
21	D[20]		
22	D[5]		
23	D[21]		
24	D[6]		
25	D[22]		
26	D[7]		
27	D[23]		
28	Ra[7]		
29	Ra[11]		Connected by zero ohm resistor
30	Vcc	+5v supply rail	Decoupled & filtered supply
31	Ra[8]		
32	Ra[9]		
33	Ras[3]*	Ndras[1] from IOMD	2nd SIMM connects to Ndras[3]
34	Ras[2]*	Ndras[0] from IOMD	2nd SIMM connects to Ndras[2]
35	Dp[2]	Parity bits - unused	4K7 pull-up on Motherboard
36	Dp[0]	Parity bits - unused	4K7 pull-up on Motherboard
37	Dp[1]	Parity bits - unused	4K7 pull-up on Motherboard
38	Dp[3]	Parity bits - unused	4K7 pull-up on Motherboard
39	Vss	0v	Connect to Digital ground
40	Cas[0]*	Ncas[0] from IOMD	
41	Cas[2]*	Ncas[2] from IOMD	
42	Cas[3]*	Ncas[3] from IOMD	
43	Cas[1]*	Ncas[1] from IOMD	
44	Ras[0]*	Ndras[0] from IOMD	2nd SIMM connects to Ndras[2]
45	Ras[1]*	Ndras[1] from IOMD	2nd SIMM connects to Ndras[3]
46	N/C		Reserved
47	We*	IOMD Nwe[0]	

Table 2.45: Pinout list for both SIMM sockets

Pin No	SIMM Signal	Description	Notes
48	N/C		Reserved
49	D[8]		
50	D[24]		
51	D[9]		
52	D[25]		
53	D[10]		
54	D[26]		
55	D[11]		
56	D[27]		
57	D[12]		
58	D[28]		
59	Vcc	+5v supply rail	Decoupled & filtered supply
60	D[29]		
61	D[13]		
62	D[30]		
63	D[14]		
64	D[31]		
65	D[15]		
66	N/C		Reserved
67	PD1	ID field from SIMM	N/C on Motherboard
68	PD2	ID field from SIMM	N/C on Motherboard
69	PD3	ID field from SIMM	N/C on Motherboard
70	PD4	ID field from SIMM	N/C on Motherboard
71	N/C		Reserved
72	Vss	0v	Connect to Digital ground

Notes:

To allow x36 bit SIMMs to be used, the parity data bits Pd[3:0] are pulled high as they are not used. Each bit has an individual pull-up.

Table 2.46: Signal timing

Parameter	Symbol	Min / Max	Value	Units
Random Read or Write Cycle	(tRC)	min	150	ns
Page Mode Read or Write Cycle	(tPC)	min	55	ns
RAS Precharge Time	(tRP)	min	55	ns
Row Address Set-up Time	(tASR)	min	0	ns
Row Address Hold Time	(tRAH)	min	12	ns
Column Address Set-up Time	(tASC)	min	0	ns
Column Address Hold Time	(tCAH)	min	20	ns
Access Time from RAS	(tRAC)	max	70	ns
Access Time from CAS	(tCAC)	max	20	ns
Access Time from CAS Precharge	(tCPA)	max	45	ns
Column Address Access Time	(tAA)	max	40	ns
RAS Pulse Width (FP Mode)	(tRASP)	min	70	ns
CAS Precharge Time (FP Mode)	(tCP)	min	20	ns
CAS to RAS Precharge Time	(tCRP)	min	20	ns
Write Command Set-up Time	(tWCS)	min	0	ns

Table 2.46: Signal timing

Parameter	Symbol	Min / Max	Value	Units
Write Command Hold Time	(tWCH)	min	15	ns
Read Command Set-up Time	(tRCS)	min	0	ns
Read Command Hold Time	(tRCH)	min	0	ns
Write Command Pulse Width	(tWP)	min	15	ns
Data in Setup Time	(tDS)	min	0	ns
Data in Hold Time	(tDH)	min	20	ns
CAS Setup Time, CBR Refresh	(tCSR)	min	10	ns
CAS Hold Time, CBR Refresh	(tCHR)	min	20	ns
Refresh Period for 1024 cycles	(tREF)	max	16	ms

Table 2.47: Capacitive loading (per SIMM)

Parameter	Min/Max	Value	Units
Ra[11:0] - Address Bus	max	128	pF
WE	max	140	pF
RAS	max	59	pF
CAS	max	59	pF
Data Bus I/O	max	29	pF

Table 2.48: Drive capability (per SIMM)

Data Bus I/O	max	171	pF

Power consumption allowance

It is possible for the Risc PC architecture to support random reads and writes to non-sequential memory locations with the cache disabled and thereby cause continued access to main memory at full system memory bandwidth; that is, continual N-cycle accesses occurring at 6.4 MHz (ie. 5 cycles of the 32MHz system clock), or 156 ns. CBR Refresh draws a similar amount of current to random read/writes and occurs at a rate of only one 160 ns cycle every 16 uS. It can not therefore affect the maximum overall current consumption by more than 1%.

The figures given below for maximum operating current are therefore directly comparable with device datasheet figures which assume the device is performing random read/writes at a minimum address cycle time (tRC) of 150 ns. These figures should be scaled accordingly if faster devices are specified at a higher rate.

Table 2.49: 5V supply (figure given per SIMM)

Maximum operating current	1300 mA
Maximum stand-by current	80 mA (inclusive of periodic refresh)

VRAM

The VRAM Module connector on the Risc PC Motherboard is a 136-way dual read-out SIMM (DIMM) connector. This allows a module to be fitted which holds either 1 or 2MB of VRAM arranged as one or two 1MB banks of 256K x 32 bits each. Suitable VRAM ICs will have a DRAM port of 256k x 8 bits, and a split transfer Serial Access Memory (SAM) port of 512 x 8 bits. Eight of these are needed for a 2MB VRAM module. Bulk and high frequency decoupling components must also be fitted to the module PCB.

Although the Risc PC platform is designed initially to support only 1 or 2 MB of VRAM there may be specialist applications for larger modules in the future. Although these would be unlikely to offer larger resolutions or colour depths due to system bandwidth limitations, it may be possible for example to provide a secondary frame buffer in a second 2 MByte bank. Support for this is provided by the addition of address line Ra<9>. Although IOMDs internal design allows it to address up to 16 MB of VRAM, only address lines Ra <9:0> are tracked to the VRAM connector and so the maximum possible address space available for VRAM is 8MB. Note that use of larger VRAM modules will require additional address mapping and control logic.

Table 2.50: Signal description

VRAM Signal	Description
Ud[31:0]	Upper Bank 32 bit SAM port data bus to VIDC Data[63:32]
Vcd[31:0]	Lower Bank 32 bit SAM port data bus to VIDC Data[31:0]
Rd[31:0]	32 bit DRAM port data bus to system data bus
Ra[9:0]	10 bit DRAM port row and column address bus from IOMD
Cas[3:0]*	4 CAS lines (both banks) for byte select within word
VRas*	RAS line to all VRAMs
We[1:0]*	Write Enable - one for each bank
Dt[1:0]*	Data Transfer & Output Enable, one for each bank
Sc	Serial Port control clock
Se*	Serial Port Enable
Dsf	Special Function input
Qsf	Special Function output
Vdd	5 Volt supply (5 Pins)
0v	Zero Volt supply - Digital ground (12 Pins)

Figure 2.17: System diagram

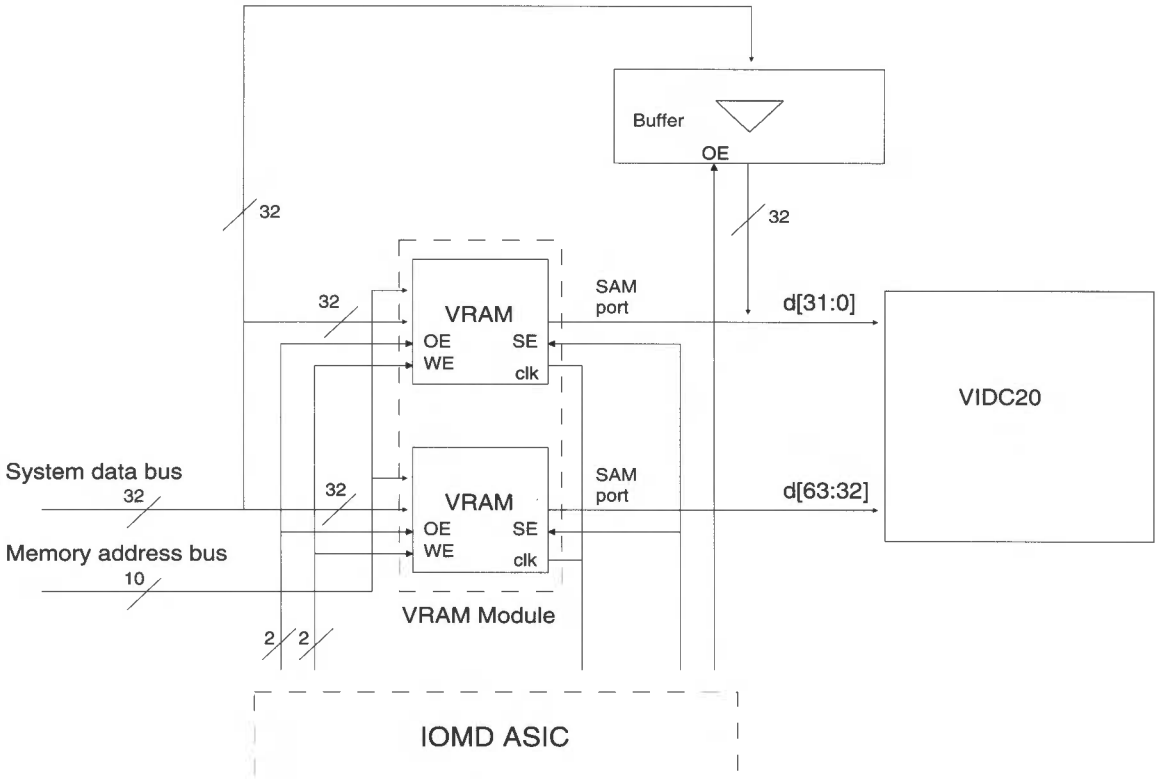


Table 2.51: Connector pinout

Pin No	Side A	Side B	Pin No	Side A	Side B
1	Ud<0>	0V	2	0V	Vcd<>
3	Ud<1>	Vcd<6>	4	Ud<2>	Vcd<5>
5	Ud<3>	+5V	6	Ud<7>	Vcd<4>
7	Vcd<0>	Rd<0>	8	Ud<6>	Rd<16>
9	Vcd<1>	Rd<1>	10	+5V	Rd<17>
11	Ud<5>	Rd<2>	12	Vcd<2>	Rd<18>
13	Ud<4>	Rd<3>	14	Vcd<3>	Rd<19>
15	Vcd<23>	0V	16	Ud<16>	Rd<22>
17	Vcd<22>	Ra<0>	18	Ud<17>	Ra<1>
19	Vcd<21>	Ra<2>	20	0V	Ra<3>
21	Ud<18>	Ra<4>	22	Vcd<20>	Ra<5>
23	Ud<19>	Ra<6>	24	Ud<23>	Ra<9>
25	Ud<22>	Rd<4>	26	Vcd<16>	Rd<20>
27	Ud<21>	Rd<5>	28	Vcd<17>	Rd<21>
29	Ud<20>	0V	30	Vcd<18>	Rd<6>
31	Vcd<19>	Rd<7>	32	0V	Rd<23>
33	Ud<15>	Ra<7>	34	Ud<14>	Ra<8>

Table 2.51: Connector pinout

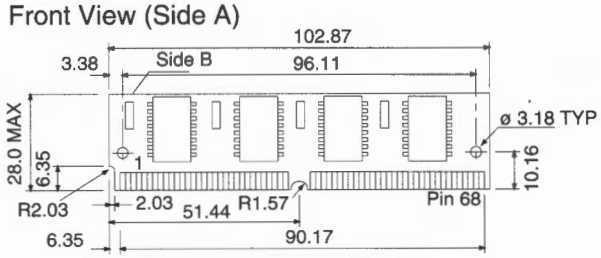
Pin No	Side A	Side B	Pin No	Side A	Side B
35	Vcd<8>	+5V	36	Ud<13>	Sc
37	Vcd<9>	Se*	38	Ud<12>	Qsf
39	Vcd<10>	Dsf	40	Vcd<11>	Cas<0>*
41	+5V	Cas<2>*	42	Vcd<15>	Cas<3>*
43	Ud<8>	Cas<1>*	44	Vcd<14>	Vras*
45	Ud<9>	Dt<0>*	46	Vcd<13>	Dt<1>*
47	Ud<10>	We<0>*	48	0V	We<1>*
49	Vcd<12>	0V	50	Ud<11>	Rd<8>
51	Vcd<24>	Rd<24>	52	Vcd<25>	Rd<9>
53	Vcd<26>	Rd<25>	54	0V	Rd<10>
55	Vcd<27>	Rd<26>	56	Ud<31>	Rd<11>
57	Ud<30>	Rd<27>	58	Ud<29>	Rd<12>
59	Ud<28>	0V	60	+5V	Rd<28>
61	Vcd<31>	Vcd<30>	62	Vcd<29>	Rd<29>
63	Vcd<28>	Rd<13>	64	Ud<24>	Rd<30>
65	Ud<25>	Rd<14>	66	Ud<26>	Rd<31>
67	Ud<27>	Rd<15>	68	0V	0V

VRAM module physical description

The VRAM Module is a double-sided PCB designed to hold Video RAM ICs on either or both sides. The PCB is inserted into the dual read-out SIMM socket (DIMM socket) on the Risc PC motherboard. The operating system recognises when the module is present and takes advantage of the extra memory bandwidth provided automatically by changing over from main DRAM.

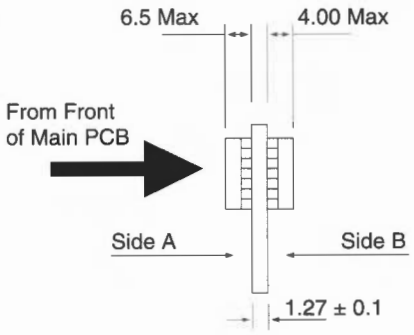
Figure 2.18: Physical dimensions and pin orientation

Front View (Side A)

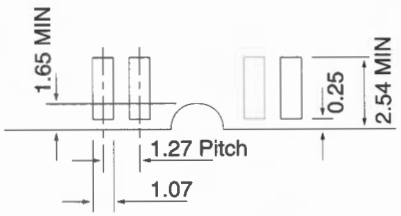


Side A Pin 1 & Side B Pin 1 are adjacent

Side View



Contact Detail



Contacts to be Gold Plated
& Centered on PCB edge

All dimensions in mm
Tolerances: ± 0.2 unless specified

The number & orientation of ICs on this module is for guidance only

Table 2.52: Signal timing
(to be observed by VRAM component ICs)

Parameter	Symbol	Min/ Max	Value	Units
Random Read or Write Cycle	(tRC)	min	150	ns
Page Mode Read or Write Cycle	(tPC)	min	55	ns
RAS Precharge Time	(tRP)	min	55	ns
Row Address Set-up Time	(tASR)	min	0	ns
Row Address Hold Time	(tRAH)	min	12	ns
Column Address Set-up Time	(tASC)	min	0	ns
Column Address Hold Time	(tCAH)	min	20	ns
Access Time from RAS	(tRAC)	max	70	ns
Access Time from CAS	(tCAC)	max	20	ns
Access Time from CAS Precharge	(tCPA)	max	45	ns
Column Address Access Time	(tAA)	max	40	ns
RAS Pulse Width	(tRAS)	min	70	ns
CAS Precharge Time (FP Mode)	(tCP)	min	20	ns
CAS to RAS Precharge Time	(tCRP)	min	20	ns
Write Command Set-up Time	(tWCS)	min	0	ns
Write Command Hold Time	(tWCH)	min	15	ns
Read Command Set-up Time	(tRCS)	min	0	ns
Read Command Hold Time	(tRCH)	min	0	ns
Write Command Pulse Width	(tWP)	min	15	ns
Data in Setup Time	(tDS)	min	0	ns
Data in Hold Time	(tDH)	min	20	ns
CAS Setup Time, CBR Refresh	(tCSR)	min	10	ns
CAS Hold Time, CBR Refresh	(tCHR)	min	20	ns
OE Access Time	(tOE)	max	25	ns
SAM port cycle time	(tSCC)	min	40	ns
Access time from SC	(tSCA)	max	25	ns
SC Precharge Time, SC Low	(tSP)	min	10	ns
Access time from SE*	(tSEA)	max	25	ns
Serial data-out hold time after SC hi	(tSOH)	min	5	ns
SC Low Hold Time after DT*	(tSDH)	min	25	ns
Split Transfer Setup Time	(tSTS)	min	70	ns
DT* to RAS* Setup Time	(tDTS)	min	0	ns
DT* to RAS* Hold Time (DT* HI)	(tDTH)	min	15	ns
DT* to RAS* Hold Time (DT* LO)	(tRDHS)	min	25	ns
DSF* to RAS* Hold Time	(tRFH)	min	15	ns
Output Disable Time From SE*	(tSEZ)	max	20	ns
Refresh Period for 512 cycles	(tREF)	max	8	ms

The above figures are given for correspondence with a typical VRAM data sheet. For example, a suitable part must operate with a minimum value of tRC no greater than 150 ns, or a maximum value of tREF which is no greater than 8 ms.

Table 2.53: Capacitive loading
(2 MB module: 8 VRAMs)

Parameter	Notes	Min/ Max	Value	Units
Address Bus: Ra[9:0]	(8 x 7 pF + tracking)	max	60	pF
Control: RAS/SC/SE/DSF	(8 x 8 pF + tracking)	max	68	pF
Control: WE/DT	(4 x 8 pF + tracking)	max	36	pF
Control: CAS	(2 x 8 pF + tracking)	max	20	pF
Data Bus: Rd[31:0]	(2 x 9 pF + tracking)	max	25	pF

Table 2.54: Drive capability

Parameter	Min/Max	Value	Units
Data Bus I/O: Rd, Vcd, Ud	min	200	pF
QSF	min	50	pF

Power consumption allowance

- DRAM port

  It is possible for the Risc PC architecture to support random reads and writes to non-sequential memory locations with the cache disabled and thereby cause continued access to main memory at full system memory bandwidth; that is, continual N-cycle accesses occurring at 6.4 MHz (ie. 5 cycles of the 32MHz system clock), or 156 ns. CBR Refresh draws a similar amount of current to random read/writes and occurs at a rate of only one 156 ns cycle every 16 uS. It can not therefore affect the maximum overall current consumption by more than 1%.

  The DRAM port figures given below for maximum operating current are therefore directly comparable with device datasheet figures which assume the device is performing random read/writes at a minimum address cycle time (tRC) of 150 ns. These figures should be scaled accordingly if devices are specified at a different minimum tRC.

- SAM port

  The SAM sends data to VIDC at a rate of 21.33 MHz (64MHz / 3). It does this when necessary to keep the video FIFO buffer full. This results in a bursty transfer. The maximum video bandwidth for the Risc PC is 160MB/s with a 2 MB VRAM system, this has a 64 bit (8 byte) wide video data bus, and is equivalent to a 20MHz (160MHz / 8) SAM clock. Therefore the current consumption for VRAM parts is specified for a cycle time of 50 ns (20 MHz). Current consumption specified for parts at a shorter cycle time than this should be scaled accordingly.

- Overall current consumption

  In a 2MB system with two banks of VRAM, although only one DRAM bank is being accessed at any one time, the other bank is still active, as they are both RAS strobed together. Furthermore, in a 2MB system, both banks of SAM will always be writing out to the screen together. Therefore, in a 2MB system, the current consumption will be two times the 1MB figure at all times.

Table 2.55: 1 MByte VRAM module at 5V (±10%) supply

Maximum operating current (DRAM Port active, SAM stand-by)	700 mA
Maximum operating current (SAM Port active, DRAM stand-by)	500 mA
Maximum stand-by current	200 mA

Thus, a 1MB VRAM module containing 4 off 256k x 8 parts would require each device to draw less than 125 mA when the SAM port is active, and less than 175 mA when the DRAM port is active.

Note. Although these figures show the SAM port to consume less power than the DRAM port, this is due to the fact that the SAM is being operated at around half it's maximum frequency whereas the DRAM port is being operated close to it's maximum.

Floppy drive

This section describes the Risc PC floppy disc interface. The interface is based around the FDC37C665 Universal Peripheral Controller from SMC (Standard Microsystems Corporation).

The interface implemented on pcb number 0197,000 supports a single PC-AT type 1MB/2MB disc drive. The interface implemented on pcb number 0197,100 supports two PC-AT type 1MB/2MB disc drives. The interface on both PCBs can be made to support an older type 5.25" disc drive by minor modifications to the floppy interface cable. The range of disc formats supported are described in the *RISC OS 3 Programmer's Reference Manual*.

There is some provision for 4MB floppy disc support in the hardware although currently the software does not fully support it, since the 4MB format seems unlikely to become widely established. The FDC37C665 itself has extensive support for the 4MB vertical recording format.

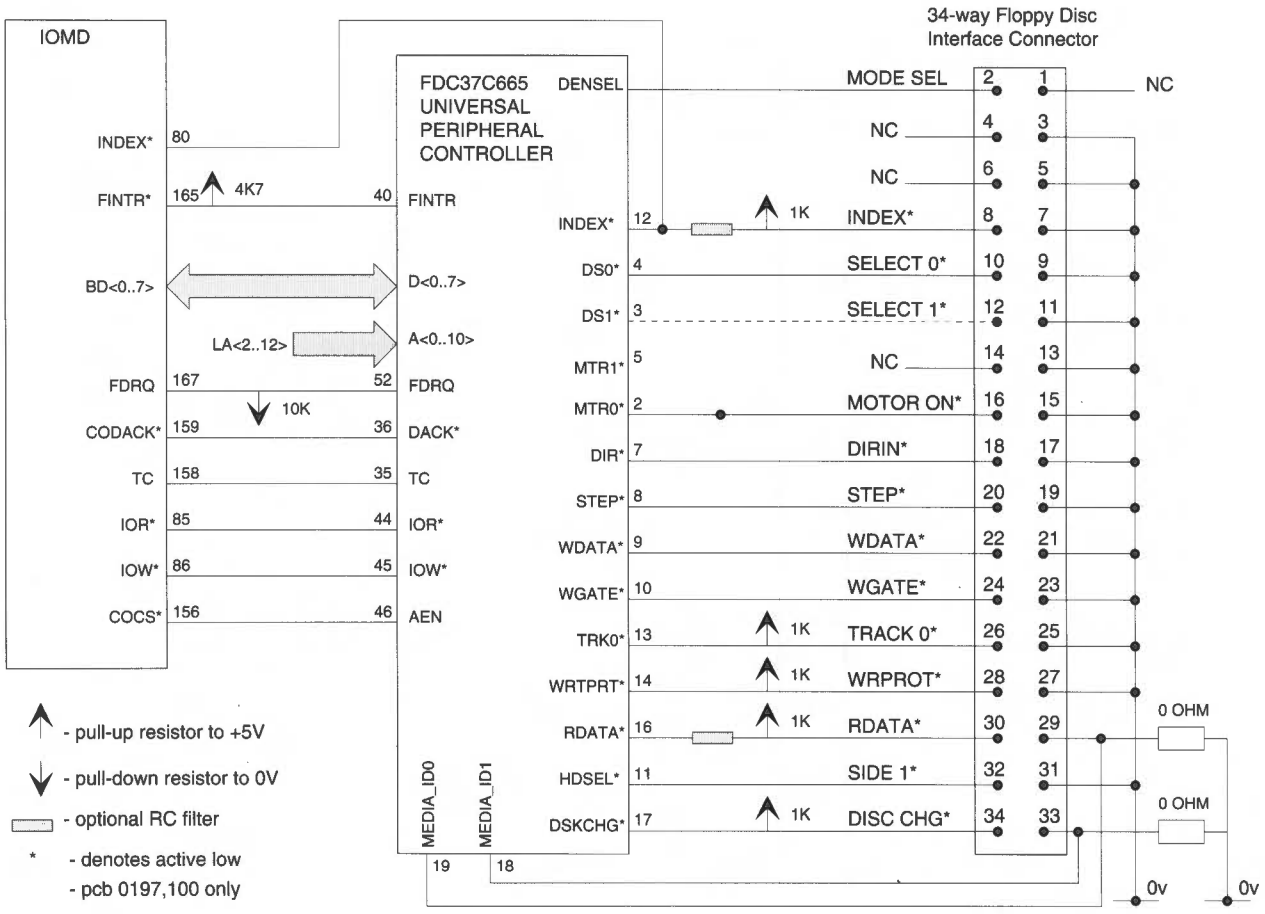
System description

The floppy disc interface hardware is integrated into the combo chip. This device contains a floppy disc controller which is software and register compatible with the Intel 82077, and utilises a '765 disc controller core. The controller uses a digital data separator requiring no external components. For a detailed description refer to SMC's datasheet *FDC37C665/FDC37C666 - Advanced High-Performance Multi-Mode Parallel Port Super I/O Floppy Disk Controllers*.

Figure 2.19 shows the floppy disc system configuration.

As on previous Acorn computers using a '765 controller (A5000, A4, A30x0 and A4000) transfer of data between the floppy disc controller and the ARM processor is by a simulated DMA mechanism using FDRQ/DACK* (Floppy DMA Request/DMA Acknowledge) handshaking. The floppy disc controller is programmed to DMA mode and the FDRQ signal from the controller is routed to IOMD which causes a FIQ (Fast Interrupt Request) to the ARM processor. The ARM responds by reading/writing a byte

Figure 2.19: Floppy disc system configuration



of data to an address in the range &0301 2000 - 0301 9FFF which causes IOMD to generate a DACK* signal. In the case of the last byte of a DMA transfer, the ARM reads/writes to the address &0302 A000 which causes IOMD to generate both a DACK* and a TC (Terminal Count) signal.

RISC OS utilises the FDC37C665's 16byte data FIFO so that events which cause long FIQ latencies do not result in data over-runs or under-runs.

IOMD is programmed to generate Type B I/O cycle timing for both the simulated DMA cycles and programmed I/O cycle to the floppy disc controller. For full details of these cycle timings see *Signal Timings* on page 2-32.

The floppy interface hardware causes 2 normal Interrupt Requests (IRQs) to the ARM processor. The first is generated by the floppy disc controller upon various controller events e.g. command completions. The second is generated by the falling edge of the INDEX* signal from the floppy drive. A set of registers within IOMD allows the interrupt sources to be controlled by the ARM processor.

Table 2.56: Signal description

Signal	Description	Drive Type
Density	Selects the floppy drive mode: '0' = 1MB '1' = 2MB	OD48
Index*	Pulses low to indicate the physical beginning of a track	IS
Drv0* Drv1*	Selects floppy drive 0 Selects floppy drive 1(on 0197,100 only)	OD48
Mtr0*	Request to rotate the drive's spindle motor	OD48
Dirin*	Indicates the direction in which the read/write heads will move when a STEP* pulse is generated: '0' = towards centre of disc '1' = towards edge of disc	OD48
Step*	Pulse low to cause the read/write heads to move in or out by one track	OD48
Writedata*	Serial bit pattern representing data to be written to the floppy disc.	OD48
Writegate*	An enable signal requesting the drive to write data onto the disc	OD48
Track0*	Indicates that the heads are positioned over Track 0 (the outermost track)	IS
Writeprot*	Indicates that a write protected disc is inserted in the drive.	IS
Readdata*	Bit pattern representing the data read from the floppy disc	IS
Side1*	Indicates which side of the disc to read from/write to: '0' = side 1 (upper) '1' = side 0 (lower)	OD48
Dskchg*	Indicates that a floppy disc has been removed from the drive	IS

Connector

The interface connector is a standard 0.1" pitch, 2-row, 34-way box header (Acorn part number 0803,102). It is strongly recommended that the cable length between the 34-way interface connector and the disc drive should not exceed 300mm.

All signals into or out of the floppy disc interface are 'open - drain'. Signals out of the floppy interface have pull-up resistors in the floppy drive itself whilst signals from the drive have pull-up resistors on the main PCB.

Pins 29 and 33 of the interface connector are connected to 0V via zero ohm resistors. These can be removed if a 4MB floppy drive is fitted so that the "MediaH" and "MediaL" outputs from the drive (on pins 29 and 33) can be routed to the FDC37C665, enabling the media type inserted in the drive to be read by software. To determine whether a 4MB floppy disc drive or a 1/2MB disc drive is fitted software reads the value of these 2 bits without selecting the drive. Note that, at the time of writing, the available 4MB disc drives are far from standardised.

Table 2.57: Connector pinout

Pin	Signal	Pin	Signal
1	nc	2	Density
4	nc	6	nc
8	Index*	10	Drv0*
12	nc (Drv1* on 0197,100)	14	nc
16	Mtr0*	18	Dirin*
20	Step*	22	Writedata*
24	Writegate*	26	Track0*
28	Writeprot*	30	Readdata*
32	Side1*	34	Dskchg*

Pins 3,5,7,9,11,13,15,17,19,21,23,25,27,29,31 & 33 are connected to 0V, (29 & 33 via zero ohm resistors).

KEY:

I	input to interface from floppy drive
O	output from interface to floppy drive
nc	no connection
*	active low signal
IS	Schmitt input
OD48	48mA output

Floppy disc power connector

Disc drive power is provided directly from the main PSU via a flying lead. The connector is a standard 4 way single-in-line polarised socket, Acorn part number 0800,930. Voltage supply details are as follows:

Table 2.58: Voltage supplies

Pin	Voltage	PSU Range	Risetime
1	+5V	4.89V - 5.2V	500ms max.
2	0V		
3	0V or nc		
4	nc		

The +5V rail rises monotonically to its specified level.

Control registers

Direct access to these registers must be avoided. This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual.*

FDC37C665 configuration registers

There are several configuration registers which can be used to configure the floppy system to various modes of operation. The FDC37C665 is programmed by RISC OS for PC-AT mode. In this mode the following registers are available at the addresses shown below:

Table 2.59: Configuration registers

Register	Address	R/W
Digital Output Reg.	&0301 0FC8	R/W
Main Status Reg.	&0301 0FD0	R
Data Rate Select Reg.	&0301 0FD0	W
Data Reg.	&0301 0FD4	R/W
Digital Input Reg.	&0301 0FDC	R
Configuration Control Reg.	&0301 0FDC	W

Full details of these registers are given in the 37C665 datasheet.

I/O timing control

This read/write register is contained within IOMD.

Table 2.60: read/write register

Register	Address	Function	Bit 3	Bit 2
I/O Timing Control Reg	&0320 00C4	Selects IOMD cycle type	T1	T0

T1 and T0 select the IOMD cycle type used for both the FDC37C665 programmed I/O and simulated DMA cycles as follows:

Table 2.61: IOMD cycle type

T1	T0	IOMD Cycle type
0	0	A
0	1	B
1	0	C
1	1	D

Interrupt registers

The following registers are contained within IOMD

Table 2.62: Interrupt registers

Register	Address	Read/Write
FIQ Interrupt Status Reg.	&0320 0030	R
FIQ Interrupt Request Reg.	&0320 0034	R
FIQ Interrupt Mask Reg.	&0320 0038	R/W
Bit 0 of these registers corresponds to the FDRQ interrupt signal.		
IRQB Interrupt Status Reg.	&0320 0020	R
IRQB Interrupt Request Reg.	&0320 0024	R
IRQB Interrupt Mask Reg.	&0320 0028	R/W
Bit 4 of these registers corresponds to the FINTR* interrupt signal.		
IRQA Interrupt Status Reg.	&0320 0010	R
IRQA Interrupt Request Reg.	&0320 0014	R
IRQA Interrupt Clear Reg.	&0320 0014	W
IRQA Interrupt Mask Reg.	&0320 0018	W
Bit 2 of these registers corresponds to the INDEX* signal.		
I/O Control Reg. (Status)	&0320 0000	R
I/O Control Reg. (Control)	&0320 0000	W
Bit 6 of these registers corresponds to the INDEX* signal.		

Interrupt status (read only)

A 1 indicates that an interrupt is pending.

A 0 indicates that there is no interrupt.

Interrupt request (read only)

A 1 indicates that an interrupt is pending and is not masked.

A 0 indicates that no interrupt is pending or the interrupt is masked, or both. This bit is the logical AND of the 'Interrupt Status' and the 'Interrupt Mask' bits.

Interrupt mask (read/write)

Writing a 0 to the 'Interrupt Mask' register disables the corresponding interrupt.

Writing a 1 enables the interrupt.

Interrupt clear (read only)

Writing a 1 to the 'Interrupt Clear' register clears the pending interrupt.

The 'I/O Control' register allows the status of the INDEX* signal to be inspected.

Other bits in the Interrupt Registers control other system interrupts and their value must be preserved at all times

For a more detailed description of these registers refer to the IOMD Functional Specification.

For further information on floppy drive operation please refer to the Acorn Component Specification *3.5" Floppy Disc Drive, read/write 2MB/1MB*, Acorn part number 0912,032/CS, which also gives full details of the performance requirements of the drive.

Signal Timings

All signal timings are referenced to TTL levels.

Table 2.63: Floppy Disc Controller Programmed I/O Cycle

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to AEN low	220			ns
t1	Address hold from AEN high	80			ns
t2	AEN select width	306	312	320	ns
t3	IOR* and IOW* strobe width	180	187	192	ns
t4	IOR* or IOW* high to AEN high	22	31	35	ns
t5	AEN low to IOR* or IOW*	90	94	100	ns
t6	IOR* or IOW* low to read data valid			100	ns
t7	Read data hold from IOR* high	10		60	ns
t8	Write data setup to IOW* high	t2			ns
t9	Write data hold from IOW* high	t4			ns
t10	IOR*/IOW* high to clear FINTR*		40	55	ns

Figure 2.20: Floppy Disc Controller Programmed I/O Cycle - IOMD Cycle Type B

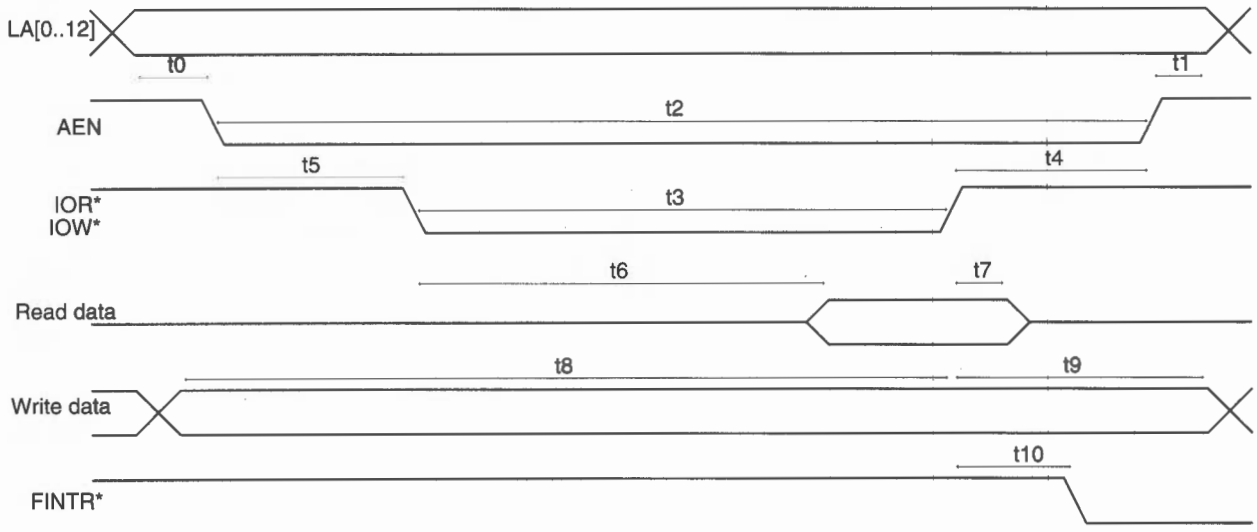


Table 2.64: Floppy Disc Controller Simulated DMA Cycle

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to DACK* low	220			ns
t1	Address hold from DACK* high	80			ns
t2	DACK* select width	306	312	320	ns
t3	IOR* and IOW* strobe width	180	187	192	ns
t4	IOR* or IOW* high to DACK* high	22	31	35	ns
t5	DACK* low to IOR* or IOW*	90	94	100	ns
t6	IOR* or IOW* low to read data valid			100	ns
t7	Read data hold from IOR* high	10		60	ns
t8	Write data setup to IOW* high	t2			ns
t9	Write data hold from IOW* high	t4			ns
t10	IOR* or IOW* low to clear FDRQ			100	ns
t11	DACK* low to clear FDRQ			100	ns
t12	TC width		312		ns

Figure 2.21: Floppy Disc Controller Simulated DMA Cycle - IOMD Cycle Type B

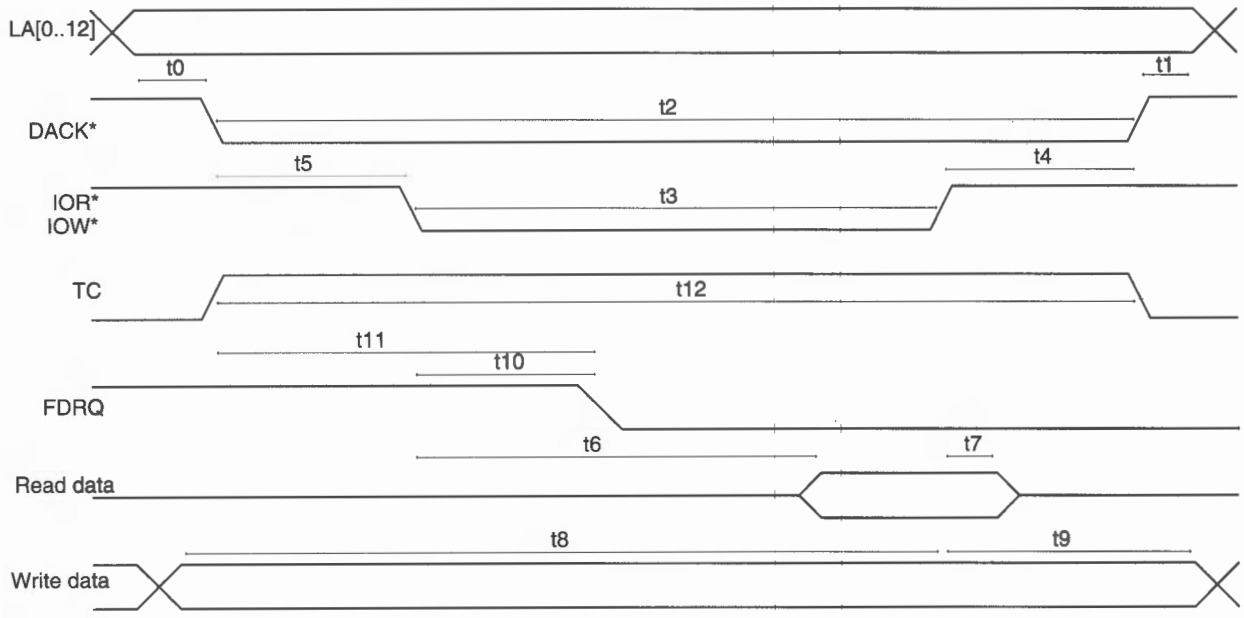


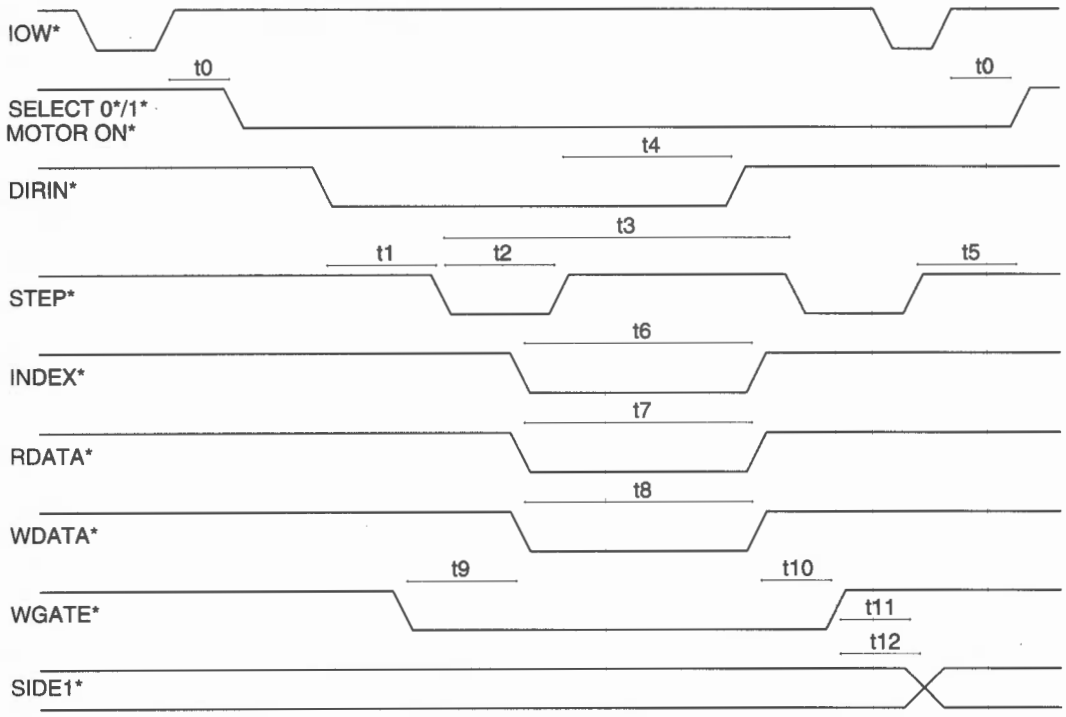
Table 2.65: Floppy disc interface timing

Sym.	Description	Min	Typ	Max	Units
t0	IOW* high to SELECT 0*/1* and MOTOR ON*		25		ns
t1	DIRIN* set up to STEP* pulse		1 (2MB) 2 (1MB)		us us
t2	STEP* pulse active low time		7 (2MB) 14 (1MB)		us us
t3	STEP* pulse cycle time	3.0			ms
t4	DIRIN* hold time after STEP*		96		X
t5	SELECT 0*/1* hold time after STEP* high		20		X
t6	Required INDEX* pulse width	2			X
t7	Required RDATA* active low time	40			ns
t8	WDATA* active low time		460 (2MB) 840 (1MB)		ns ns
t9	WGATE* low to first WDATA* pulse		2.5 (2MB) 4.5 (1MB)		us us
t10	last WDATA* pulse to WGATE* high		2.4 (2MB) 5.0 (1MB)		us us
t11	WGATE* to STEP* †	436 (2MB) 664 (1MB)			us us
t12	WGATE* to SIDE1* †	360 (2MB) 492 (1MB)			us

X = 25ns for 500kbps (2MB) datarate
250ns for 250kbps (1MB) datarate

† measured for a 25MHz ARM700

Figure 2.22: Floppy disc interface timing



Programmable timing parameters

Several timing parameters of the floppy disc interface signals are programmable within the FDC37C665 as described below.

Write Precompensation

Precompensation is programmed to occur on all tracks and is set to the following values:

Table 2.66: Write precompensation

Data Rate	Precompensation
500Kbps	125ns
250Kbps	125ns

Step Rate

The Step Rate Interval defines the time between successive step pulses. It can be configured by the user using the *CONFIGURE STEP command as follows:

Table 2.67: Step rate

	Actual step rate (ms)	
Configured step rate	250Kbps	500Kbps
2	2	2
3	4	3
6	6	6
12	26	12

Disc Formats

The FDC37C665 can be programmed to format discs with various sector sizes, gaps etc. In all cases it generates an Index Address field following the physical INDEX* pulse.

IDE - hard disc

The Risc PC IDE (Integrated Drive Electronics) interface is a PC-AT compatible interface. It is virtually identical in terms of hardware and software to the Acorn A5000 IDE interface. The interface supports up to 2 IDE drives (referred to as Master and Slave drives) and these are daisy-chained together on the IDE interface cable. Power is available via two standard 4-way sockets, one of which is connected to the hard disc fitted as standard.

An IDE drive has all the disc controller circuitry integrated into the drive itself, thus providing a very simple interface to the computer. An official standard describing both hardware and software aspects of the interface has been published by the CAM (Common Access Method) Committee as the interface is now commonplace in the PC industry. Like SCSI, it is a logic-level interface and drives accept high-level commands (eg. Read Sector), generating an interrupt on completion of each command. Being intelligent, IDE drives possess features which result in faster operation and more efficient data storage. For example, many have a buffer memory which they use to cache several sectors of data during reads and writes. The Acorn IDE driver software adheres as closely as possible to the CAM recommendations. However, it does not currently implement any of the multiple commands allowing multiple sector operations within a single interrupt.

This specification refers throughout to the use of an SMC 37C665 Universal Peripheral Controller since this is the device used on the Issue 1 Risc PC PCB part numbers 0197,000 and 0197,100. Use of a different combo device will not affect the functionality of the IDE interface described in this document, although some interface timings may be different and the register descriptions will be inapplicable.

If attempting to interface a slave drive, you should refer to

- the Acorn IDE drive component specifications listed on page 2-38, which provide specifications for suitable slave drives
- the relevant drive manual which explains how to set the appropriate ID links on the slave.

Full details of the IDE master slave standard appear in ATA/CAM Specification (BSR X3.221, X3T9.2/90-143).

Table 2.68: Floppy interface electrical characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Condition
All input signals (type IS)						
Low-level input voltage	V_{IL}			0.8	V	V_{CC} = 5.0v
High-level input voltage	V_{IH}	2.2			V	
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
Low-level input current	I_L	-4.7		-5.5	mA	V_{IN} = 0V
All output signals (type OD48)						
Low-level output voltage	V_{OL}			0.4	V	I_{0L} = -48mA
Output leakage current	I_{OH}	-10		+10	uA	V_{0H} = 0 to V_{CC}

System description

All accesses to the IDE drive are by programmed I/O and are controlled by IOMD which is programmed to generate Type B I/O cycle timing as shown below. Register accesses are 8 bits wide whereas data transfers are 16 bits. IOMD also contains the IDE interrupt control logic. An IDE interrupt causes a normal Interrupt Request (IRQ) to the ARM processor.

The interface is jointly controlled by IOMD and the FDC37C665 Peripheral Controller.

The FDC37C665 contains the IDE address decode logic and provides enable signals for the bi-directional data buffers. It also connects data bit 7 of the IDE drive to data bit 7 of the Risc PC buffered data bus during IDE drive register accesses, except in the case of a read from the Drive Address register, when it drives data bit 7 of the data bus with a value reflecting the state of the floppy disc 'Disc Changed' line.

The IDE drives fitted as standard on the Risc PC have the following performance parameters:

Table 2.69: IDE drives performance parameters

Performance parameter	210MB	420MB
Power supply	+5V (±5%) +12V (±5%)	+5V (±5%) +12V (±5%)
Average seek time	14ms	14ms
Track to track seek time	3.0ms	3.0ms
Non-recoverable read error rate	<1 in 10E14	<1 in 10E14
Power consumption (typical read/write)	3.7W	3.7W

Figure 2.23: Block diagram of the IDE interface

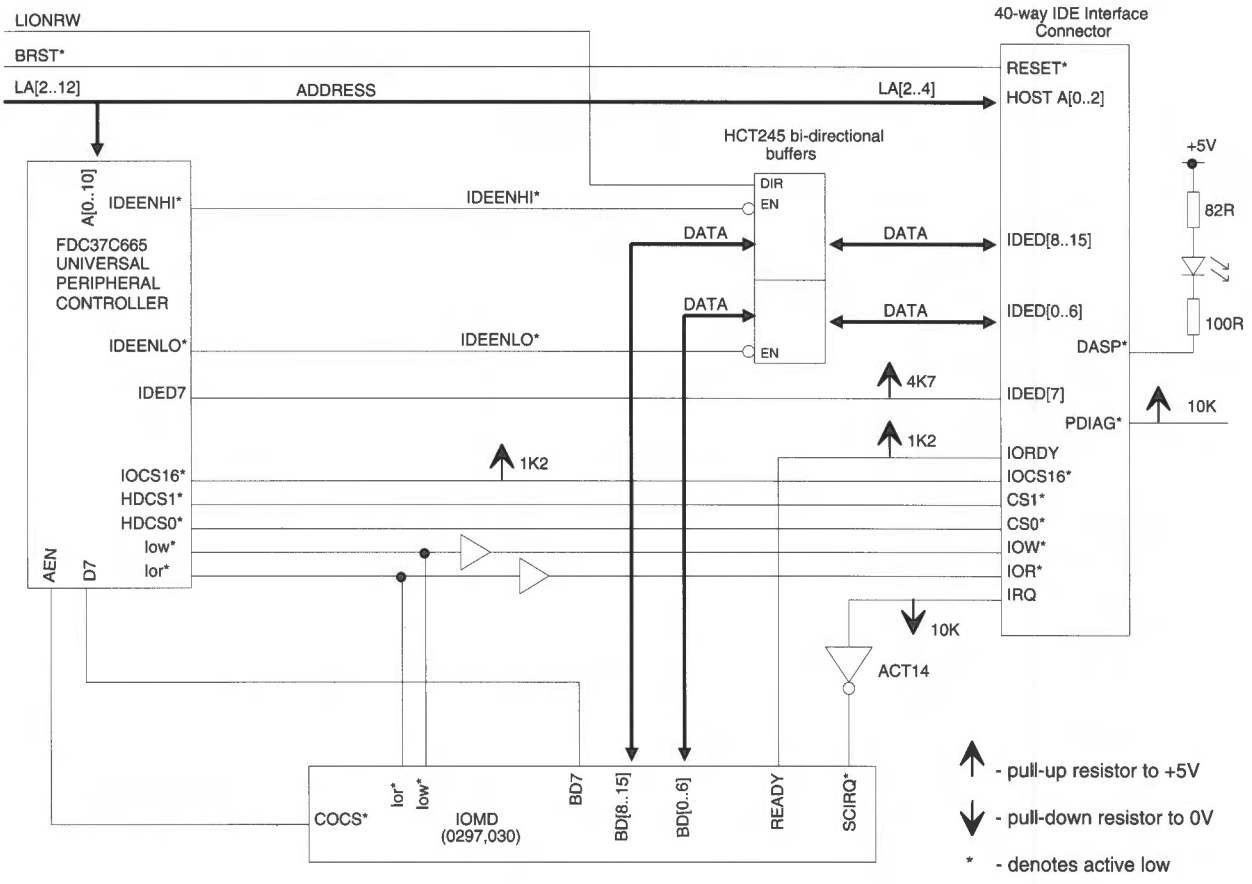


Table 2.70: Signal description

Signal	Description	Drive Type
RESET*	Reset signal from IOMD	O4
IDED[15:0]	16 Bit bi-directional, tri-state data bus	IT/O6Z, (bit 7 is IT/O24TZ)
HOST A[2:0]	3 Bit IDE address line.	O8
IOW*	I/O Write strobe; rising edge strobes host data into IDE drive	O8
IOR*	I/O Read strobe; falling edge enables data from IDE drive	O8
IORDY	I/O Ready - used to extend I/O cycles ③	IS
IRQ	Interrupt request to host system (active high)	IT
IOCS16*	Indicates that the IDE Data Register has been addressed	IT
CS{1:0}*	IDE drive select lines.	O10T
PDIAG*	Slave Passed Diagnostics ①	IT
DASP*	IDE Activity / Slave present line ②	IT
0V	Ground to motherboard and IDE drive	

Connector

The interface connector is a standard 0.1" pitch, 2 row, 40-way box header (Acorn part number 0 803,103). It is strongly recommended that the total cable length between the 40-way interface connector and the disc drive(s) should not exceed 250mm.

Table 2.71: Connector pinout

Pin	Signal	Pin	Signal
1	RESET*	2	0V
3	IDED[7]	4	IDED[8]
5	IDED[6]	6	IDED[9]
7	IDED[5]	8	IDED[10]
9	IDED[4]	10	IDED[11]
11	IDED[3]	12	IDED[12]
13	IDED[2]	14	IDED[13]
15	IDED[1]	16	IDED[14]
17	IDED[0]	18	IDED[15]
19	0V	20	nc ⑤
21	nc	22	0V
23	IOW*	24	0V
25	IOR*	26	0V
27	IORDY	28	nc ④
29	nc	30	0V
31	IRQ	32	IOCS16*
33	HOST A[1]	34	PDIAG*
35	HOST A[0]	36	HOST A[2]
37	CS0*	38	CS1*
39	DASP*	40	0V

KEY

nc	no connection.
*	active low signal.
IT	TTL level input.
IS	Schmitt input.
O4	4mA output.
O6Z	6mA CMOS level tri-state output.
O8	8mA CMOS level output.
O24TZ	24mA TTL level tri-state output.
O10T	10mA TTL level output.
①	This line is asserted by the Slave drive to inform the Master drive that the Slave has passed its internal diagnostic routine and is ready to accept commands from the host. It does this following a hard or soft reset and on completing an 'Execute Drive Diagnostics' command. In driving this line, the Slave must conform to the timing parameters laid down in the ATA/CAM Specification.
②	This line is asserted by the Slave drive following a hard reset to inform the Master drive that the Slave is present. After reset this line is driven by either the Master or the Slave to drive the disc activity LED on the Risc PC front panel. In driving this line, the Master and Slave must conform to the ATA/CAM timing parameters. Failure to do so will result in incorrect Slave operation.
③	Drives that do not use IORDY must satisfy a minimum read/write cycle time of 500ns sustained over a complete sector.
④	Drives using this pin as 'Spindle Sync' or 'Cable Select' must have this feature disabled.
⑤	On an IDE drive the corresponding pin is usually removed and used as a 'key' to guarantee correct orientation of IDE cable.

IDE Power connector

IDE drive power is provided directly from the main PSU via a flying lead. The connector is a standard 4 way socket housing with crimped terminal pins (Acorn part numbers 0800,504 and 0800,500 respectively). Voltage supply details are as follows:

Table 2.72: Voltage supplies

Pin	Voltage	PSU Range	Risetime
1	+12V	11.4V - 12.6V	500ms max
2	0V (+12V return)	-	
3	0V (+5V return)	-	
4	+5V	4.89V - 5.2V	500ms max

The +5V and +12V rails rise monotonically to their specified levels within 10ms of each other.

Control registers

Direct access to these registers must be avoided. This section is for information only and is subject to change. All access should be via the RISC OS software interfaces defined in the *RISC OS 3 Programmer's Reference Manual*.

I/O Timing control

This read/write register is within IOMD.

Table 2.73: I/O Timing control register

Register	Address	Function	Bit3	Bit2
I/O Timing Control	&0320 00C4	Selects IOMD cycle type	T1	T0

T1 and T0 select the IOMD cycle type used for the FDC37C665 and IDE drive I/O read/write cycles as follows:

Table 2.74: IOMD cycle types

T1	T0	IOMD Cycle type
0	0	A
0	1	B
1	0	C
1	1	D

Interrupt Registers

These registers are contained within IOMD.

Table 2.75: Interrupt registers

Register	Address	Read/Write	Bit 1
IRQB Interrupt Status	&0320 0020	R	SCIRQ*
IRQB Interrupt Request	&0320 0024	R	SCIRQ*
IRQB Interrupt Mask	&0320 0028	R/W	SCIRQ*

Interrupt status (read only)

A 1 indicates that an interrupt is pending (i.e. SCIRQ* is logic '0').

A 0 indicates that there is no interrupt.

Interrupt request (read only)

A 1 indicates that an interrupt is pending and is not masked.

A 0 indicates that no interrupt is pending or the interrupt is masked, or both. This bit is the logical AND of the 'Interrupt Status' and the 'Interrupt Mask' bits.

Interrupt mask (read/write)

Writing a 0 to the Interrupt Mask register disables the corresponding interrupt.

Writing a 1 enables the interrupt.

Other bits in the Interrupt Registers control other system interrupts and their values must be preserved at all times. For a more detailed description of these registers refer to the IOMD Functional Specification.

FDC37C665 registers

There are two Configuration Registers within the FDC37C665 which can be used to configure the IDE interface:

Table 2.76: Configuration registers

Register	Read/Write	Bit 1	Bit 0
Configuration Reg. 0	R/W	IDE AT/XT	IDE EN
Configuration Reg. 5	R/W	IDE SEC	

Configuration Register 0 enables and disables the IDE interface and selects between either a PC-XT or PC-AT interface.

Configuration Register 5 selects the Primary and Secondary addresses for the IDE interface registers.

Within the Risc PC IDE system the primary address is used and a PC-AT interface is selected and enabled. Full details of these registers and how to access them are available in the FDC37C665 datasheet.

IDE drive registers

The IDE drive contains several registers which reside at addresses determined by the Risc PC address decoding and the selection of primary IDE address using Configuration Register 5 (described above). These are listed below:

Table 2.77: IDE drive registers

Address	Read	Write
&0301 07C0	Data register	Data register
&0301 07C4	Error register	Write Precomp register
&0301 07C8	Sector count	Sector count
&0301 07CC	Sector number	Sector number
&0301 07D0	Cylinder low	Cylinder low
&0301 07D4	Cylinder high	Cylinder high
&0301 07D8	SDH register	SDH register
&0301 07DC	Status register	Command register
&0301 0FD8	Alt. status register	Dig. output register
&0301 0FDC	Drive address reg.	Not used

When the Drive address register is read the FDC37C665 drives bit 7 of the host data bus with a value that reflects the status of the 'Disc Changed' bit of the floppy disc interface.

For a more detailed description of the IDE drive registers refer to the IDE drive manual, as these are drive specific.

For further information on IDE drive operation please refer to the Acorn Component Specifications:

- *Hard Disc Drive 210MB Formatted – 3.5" Low Profile Footprint IDE interface*
  Acorn part number 0912,030/CS
- *Hard Disc Drive 420MB Formatted – 3.5" Low Profile Footprint IDE interface*
  Acorn part number 0912,031/CS

These also give full details of the performance requirements of the drive.

Signal timings

Table 2.78: IDE data register read (16-bit)

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to LIONRW		0		ns
t1	Address setup to AEN	220			ns
t2	AEN low to IDE drive select, CS0*		10	40	ns
t3	AEN low to IOR*	90	94	100	ns
t4	AEN select width	306	312	320	ns
t5	Address hold from AEN high	80			ns
t6	AEN high to CS0* delay		10	40	ns
t7	IOR* high to AEN high	22	31	35	ns
t8	IORDY pulse width	0		1250	ns
t9	Allowable IOR* to IORDY delay	0		35	ns
t10	Allowable IOR* low to read data valid	0		85	ns

Table 2.78: IDE data register read (16-bit)

Sym.	Description	Min	Typ	Max	Units
t11	Allowable IDE read data hold from IOR* high	5		60	ns
t12	Data bit 7 hold from IOR* high	10		60	ns
t13	IOR* strobe width	180	187	192	ns
t14	Data bit 7 delay	10		60	ns
t15	Allowable CS0* to IOCS16* delay			20	ns
t17	AEN low to IDEENLO* delay			40	ns
t18	IOCS16* low to IDEENHI* delay			40	ns
t19	data buffer delay		12	35	ns
t20	AEN high to IDEENLO* delay			40	ns
t21	AEN high to IDEENHI* delay			40	ns
t22	data buffer disable time		15	45	ns
t23	IOR* high to IOCS16* high	5			ns

Figure 2.24: IDE data register read (16-bit) - IOMD cycle type B

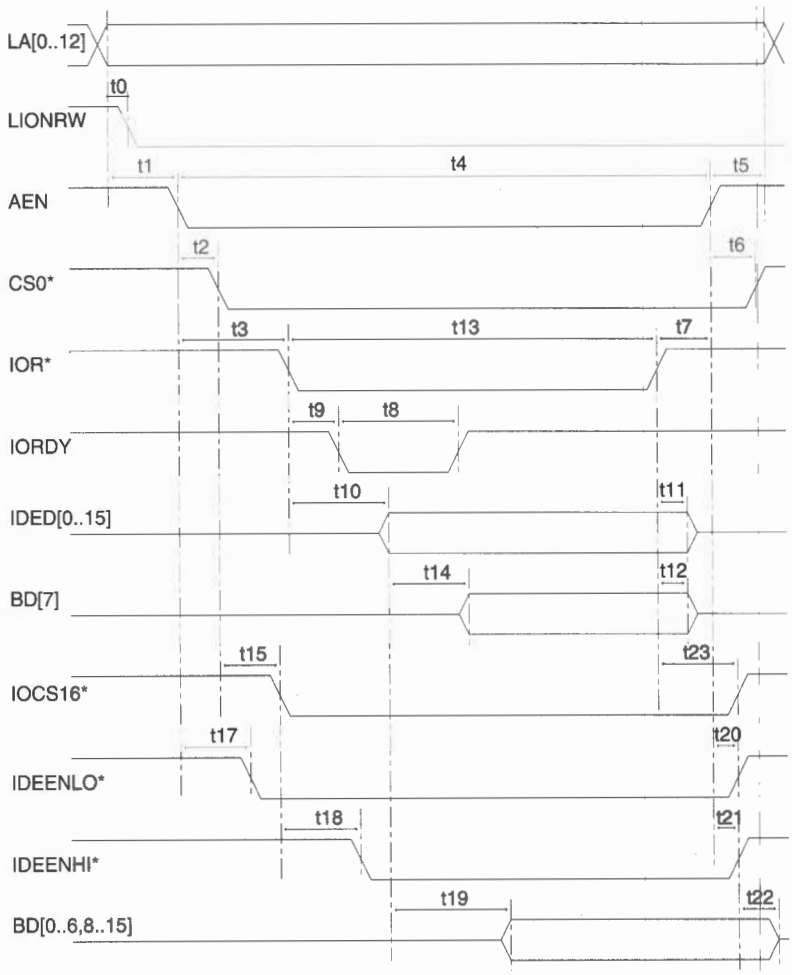


Table 2.79: IDE data register write (16-bit)

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to LIONRW		0		ns
t1	Address setup to AEN	220			ns
t2	AEN low to IDE drive select, CS0*		10	40	ns
t3	AEN low to IOW*	90	94	100	ns
t4	AEN select width	306	312	320	ns
t5	Address hold from AEN high	80			ns
t6	AEN high to CS0* delay		10	40	ns
t7	IOW* high to AEN high	22	31	35	ns
t8	Allowable IORDY pulse width	0		1250	ns
t9	Allowable IOW* to IORDY delay	0		35	ns
t10	data buffer enable time		15	45	ns

Table 2.79: IDE data register write (16-bit)

Sym.	Description	Min	Typ	Max	Units
t11	data buffer disable time		15	45	ns
t12	IDED[7] hold from IOW* high	10		50	ns
t13	IOW* strobe width	180	187	192	ns
t14	IDED[7] delay from IOW* low			50	ns
t15	Allowable CS0* to IOCS16* delay			20	ns
t17	AEN low to IDEENLO* delay			40	ns
t18	IOCS16* low to IDEENHI* delay			40	ns
t20	AEN high to IDEENLO* delay			40	ns
t21	AEN high to IDEENHI* delay			40	ns
t22	IOW* high to IOCS16* high	5			ns

Figure 2.25: IDE data register write (16-bit) - IOMD cycle type B

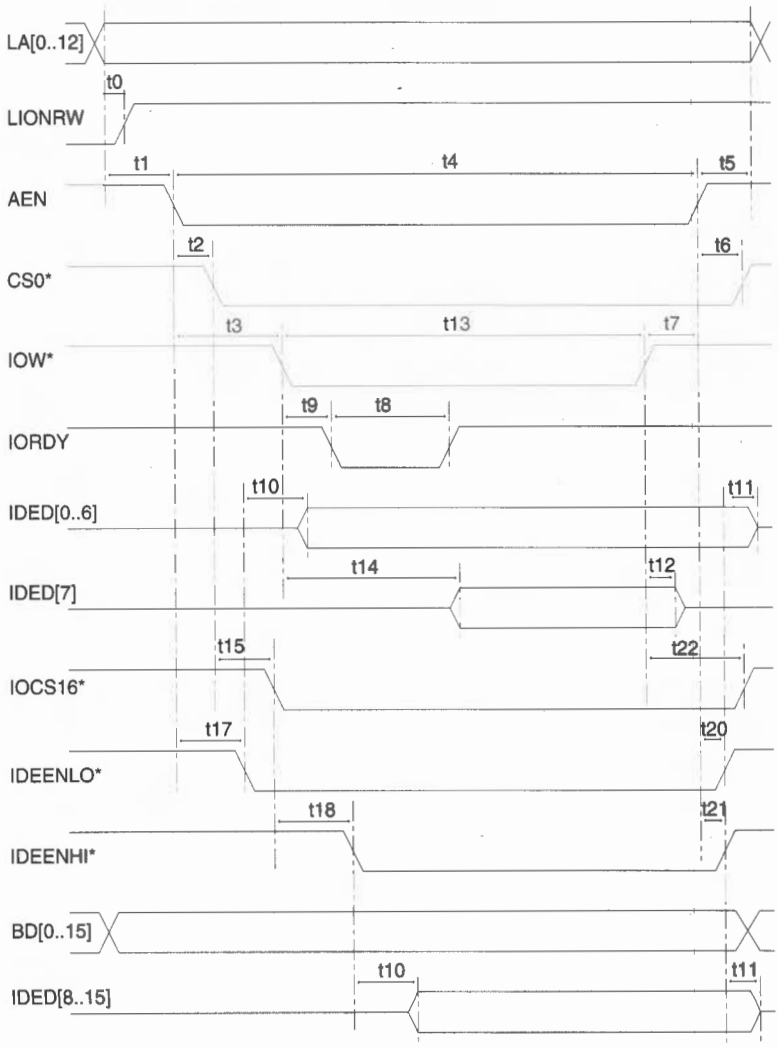


Table 2.80: IDE data register read (8-bit)

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to LIONRW		0		ns
t1	Address setup to AEN	220			ns
t2	AEN low to IDE drive select, CS0*		10	40	ns
t3	AEN low to IOR*	90	94	100	ns
t4	AEN select width	306	312	320	ns
t5	Address hold from AEN high	80			ns
t6	AEN high to CS0* delay		10	40	ns
t7	IOR* high to AEN high	22	31	35	ns
t8	IORDY pulse width	0		1250	ns
t9	Allowable IOR* to IORDY delay	0		35	ns
t10	Allowable IOR* low to read data valid	0		85	ns
t11	Allowable IDE read data hold from IOR* high	5		60	ns

Table 2.80: IDE data register read (8-bit)

Sym.	Description	Min	Typ	Max	Units
t12	Data bit 7 hold from IOR* high	10		60	ns
t13	IOR* strobe width	180	187	192	ns
t14	Data bit 7 delay	10		60	ns
t15	Allowable CS0* to IOCS16* delay			20	ns
t17	AEN low to IDEENLO* delay			40	ns
t18	IOCS16* low to IDEENHI* delay			40	ns
t19	data buffer delay		12	35	ns
t20	AEN high to IDEENLO* delay			40	ns
t21	AEN high to IDEENHI* delay			40	ns
t22	data buffer disable time		15	45	ns

Figure 2.26: IDE data register read (8-bit) - IOMD cycle type B

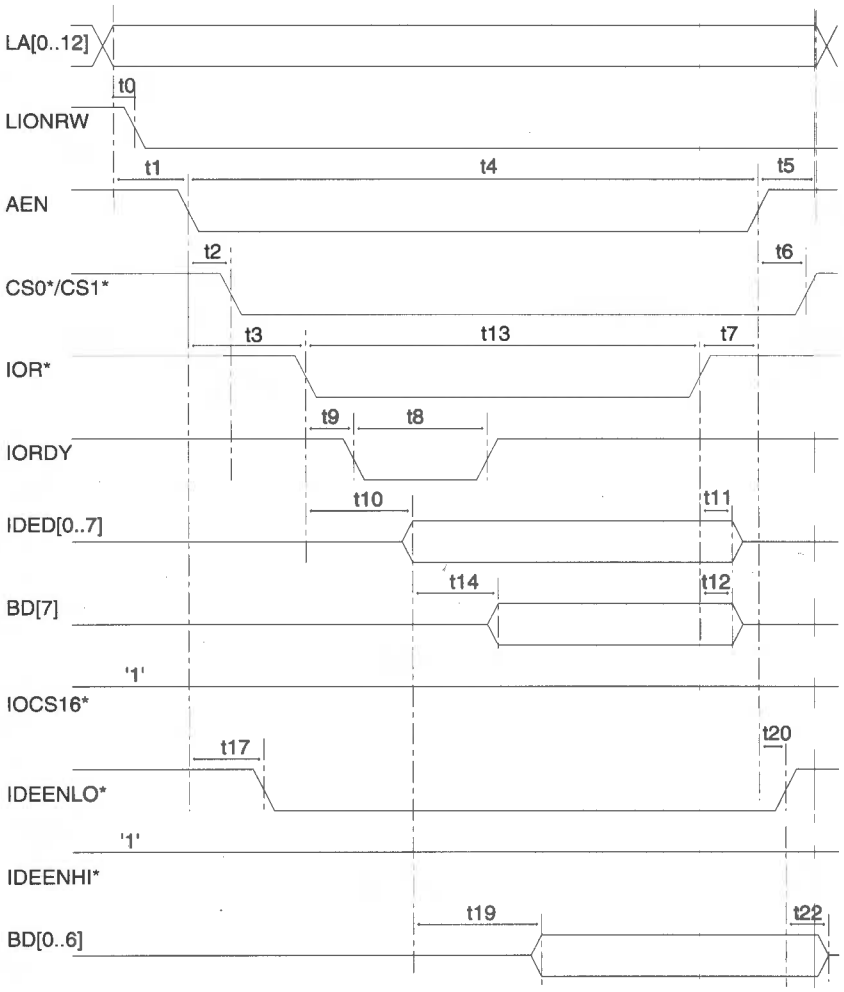


Table 2.81: IDE data register write (8-bit)

Sym.	Description	Min	Typ	Max	Units
t0	Address setup to LIONRW		0		ns
t1	Address setup to AEN	220			ns
t2	AEN low to IDE drive select, CS0*		10	40	ns
t3	AEN low to IOW*	90	94	100	ns
t4	AEN select width	306	312	320	ns
t5	Address hold from AEN high	80			ns
t6	AEN high to CS0* delay		10	40	ns
t7	IOW* high to AEN high	22	31	35	ns
t8	Allowable IORDY pulse width	0		1250	ns
t9	Allowable IOW* to IORDY delay	0		35	ns

Table 2.81: IDE data register write (8-bit)

Sym.	Description	Min	Typ	Max	Units
t10	data buffer enable time		15	45	ns
t11	data buffer disable time		15	45	ns
t12	IDED[7] hold from IOW* high	10		50	ns
t13	IOW* strobe width	180	187	192	ns
t14	IDED[7] delay from IOW* low			50	ns
t15	Allowable CS0* to IOCS16* delay			20	ns
t17	AEN low to IDEENLO* delay			40	ns
t18	IOCS16* low to IDEENHI* delay			40	ns
t20	AEN high to IDEENLO* delay			40	ns
t21	AEN high to IDEENHI* delay			40	ns

Figure 2.27: IDE data register write (8-bit) - IOMD cycle type B

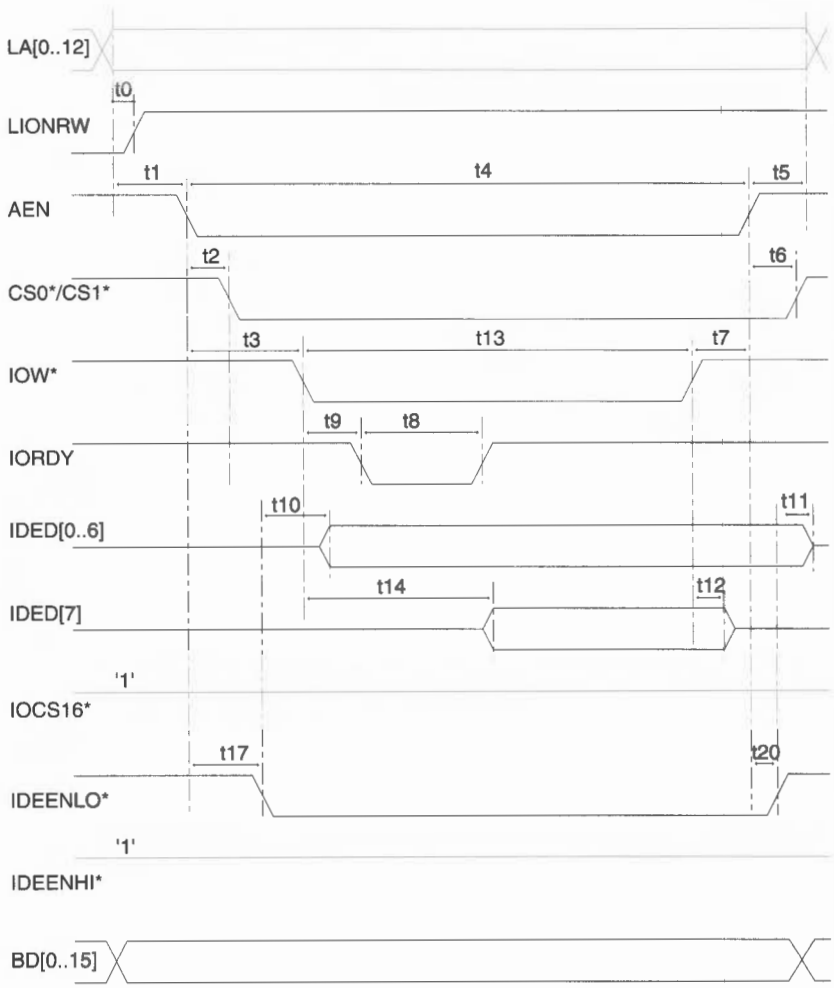
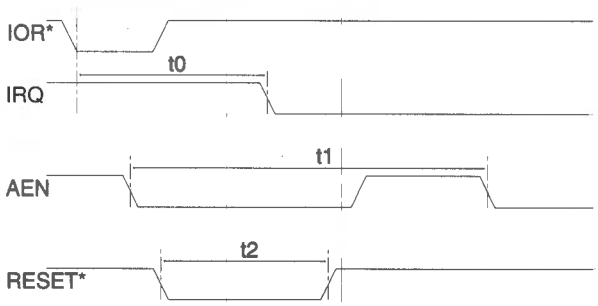


Table 2.82: Other IDE timings

Sym.	Description	Min	Typ	Max	Units
t0	IOR* low to clear IRQ		650		ns
t1	Minimum AEN cycle time		750		ns
t2	Reset pulse width	50			ms

Figure 2.28: Other IDE timings



Electrical characteristics

Table 2.83: Input signal drive types

Input Signal Drive Types	Symbol	Min	Typ	Max	Units	Test Condition
Type IS Low-level input voltage	V_{IL}		0.8	V	V_{CC} = 5.0V	
High-level input voltage	V_{IH}	2.2		V		
Low-level input current	I_L	-4.0		-4.4	mA	V_{IN} = 0V
High-level input leakage	I_H	-10		+10	uA	V_{IN} = V_{CC}
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
Type IT Low-level input voltage	V_{IL}		0.8	V	V_{CC} = 5.0V	
High-level input voltage	V_{IH}	2.0		V		

Table 2.84: Output signal drive types

Output Signal Drive Types	Symbol	Min	Typ	Max	Units	Test Condition
Type O4 Low-level output voltage	V_{OL}			0.4	V	I_{0L} = -4mA, V_{CC} = 4.5V
High-level output voltage	V_{OH}	3.7			V	I_{OH} = 4mA, V_{CC} = 4.5V
Output leakage current	I_{OH}	-10		+10	uA	V_{0H} = 0 to V_{CC}
Type O6Z Low-level output voltage	V_{OL}			0.4	V	I_{0L} = -6mA, V_{CC} = 4.5V
High-level output voltage	V_{OH}	3.7			V	I_{OH} = 6mA, V_{CC} = 4.5V
Output leakage current	I_{OH}	-10		+10	uA	V_{0H} = 0 to V_{CC}
Type O8 Low-level output voltage	V_{OL}			0.55	V	I_{0L} = -8mA, V_{CC} = 4.5V
High-level output voltage	V_{OH}	3.9			V	I_{OH} = 8mA, V_{CC} = 4.5V
Output leakage current	I_{OH}	-5		+5	uA	V_{0H} = 0 to V_{CC}
Type O10T Low-level output voltage	V_{OL}			0.5	V	I_{0L} = -10mA
High-level output voltage	V_{OH}	2.4			V	I_{OH} = 10mA
Output leakage current	I_{OH}	-10		+10	uA	V_{0H} = 0 to V_{CC}
Type O24TZ Low-level output voltage	V_{OL}			0.4	V	I_{0L} = -24mA
High-level output voltage	V_{OH}	2.4			V	I_{OH} = 12mA
Output leakage current	I_{OH}	-10		+10	uA	V_{0H} = 0 to V_{CC}

Links, plugs and sockets

Table 2.85: Links

Link	Fitted	Description	
LK1	No	2 Way	Processor Address A[29:28]
LK2	No	6 Way	IOMD Boundary Scan
LK3	No	5 Way	Sound CODEC Interface from IOMD
LK4	Yes	6 Way	Power On Self Test
LK5	Yes	3 Way	CMOS Write Protection
LK6	No		Gnd point for VIDC
LK7	No	6 Way	VIDC20 Boundary Scan
LK8	Yes	6 Way	VIDC20 16 bit serial sound output
LK9	No		Gnd point for VIDC
LK10	No		Gnd point for VCO
LK11	Yes	2 Way	Speaker
LK12	Yes	4 Way	Power & Disc activity LEDs
LK13	Yes	10 Way	Auxiliary Audio Connector A
LK14	Yes	5 Way	Auxiliary Audio Connector B

Table 2.86: Plugs

Plug	Fitted	Description	
PL1	Yes	9 Way	Serial
PL2	Yes	34 Way	Floppy
PL3	Yes	40 Way	IDE
PL4	Yes	6 Way	Power In
PL5	Yes	16 Way	Video Feature & Genlock

Table 2.87: Sockets

Socket	Fitted	Description	
SK1	Yes	96 Way	OPEN Bus - ARM CPU
SK2	Yes	96 Way	OPEN Bus - 2nd CPU
SK3	Yes	25 Way	Parallel Port
SK4	Yes	48 Way	Network
SK5	Yes	9 Way	Mouse Port
SK6	Yes	72 Way	DRAM SIMM 0
SK7	Yes	72 Way	DRAM SIMM 1
SK8	Yes	6 Way	Keyboard
SK9	Yes	136 Way	VRAM DIMM
SK10	Yes	15 Way	Monitor
SK11	Yes	132 Way	DEBI Podule Bus
SK12	Yes	–	Headphone / Stereo out

Part 3 – Parts lists

Risc PC main PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,000	BARE PCB	1	
2	0197,000/A	PCB ASSEMBLY DRG		1 Per Batch.
3	0197,000/C	PCB CIRCUIT DIAGRAM		1 Per Batch.
4				
5	0297,082	PANEL REAR - MAIN PCB	1	
6				
7	0800,070	CONR 2W SHUNT 0.1"	3	Use on LK5 (Pins 1 to 2), LK14 (Pins 1 to 2, 3 to 4)
9				
10	0800,951	CONRD 4-4O SEMS SCWLK 5L	6	Use on SK3, SK10, PL1
11	0870,420	WIRE 22SWG CPR TIN	A/R	Use on X3.
12	0880,200	SLVING 1,02mmID PTFE	A/R	Use on X3.
13				
14	0884,039	RIVET POP 3/32"D FOR 64W	6	Use on SK1, SK2, SK4.
	0884,036	RIVET PLST SNAP 4,5THK		Option
16				
17	0895,085	ADH PAD 6x4x1thkmm DSD	1	Use under BT1.
	0902,013	LABEL 6,4mmD D/Grn/SA PCB		Option
19				
20	0902,014	LABEL PCB SERIAL No 40x10	1	
21	0800,102	SKT IC 42/0.6" SUPA	1	IC14
22	0800,102	SKT IC 42/0.6" SUPA	1	IC15
23	0800,197	SKT STRIP 3/0.1" TURN	1	IC17
BT1	0817,016	BAT NH 1V2 280MAH VT HT	1	
C1	0693,336	CPCTR 33N DCPLR SMD 805	1	
C2	0635,230	CPCTR 220U ALEC 16V RAD	1	
C3	0693,336	CPCTR 33N DCPLR SMD 805	1	
C4	0693,336	CPCTR 33N DCPLR SMD 805	1	
C5	0693,336	CPCTR 33N DCPLR SMD 805	1	
C6	0690,680	CPCTR 68P CML 2% 0805	1	
C7	0690,120	CPCTR 12P CML 2% 0805	1	
C8	0690,101	CPCTR 100P CML 2% 0805	1	
C9	0693,336	CPCTR 33N DCPLR SMD 805	1	
C10	0693,336	CPCTR 33N DCPLR SMD 805	1	
C11	0690,101	CPCTR 100P CML 2% 0805	1	
C12	0681,101	CPCTR 10U TANT SMD 16V	1	
C13	0690,101	CPCTR 100P CML 2% 0805	1	
C14	0693,336	CPCTR 33N DCPLR SMD 805	1	
C15	0693,336	CPCTR 33N DCPLR SMD 805	1	
C16	0690,101	CPCTR 100P CML 2% 0805	1	
C17	0693,336	CPCTR 33N DCPLR SMD 805	1	
C18	0693,336	CPCTR 33N DCPLR SMD 805	1	
C19	0690,101	CPCTR 100P CML 2% 0805	1	
C20	0693,336	CPCTR 33N DCPLR SMD 805	1	
C21	0690,101	CPCTR 100P CML 2% 0805	1	
C22	0690,101	CPCTR 100P CML 2% 0805	1	
C23	0690,680	CPCTR 68P CML 2% 0805	1	
C24	0693,336	CPCTR 33N DCPLR SMD 805	1	
C25	0690,101	CPCTR 100P CML 2% 0805	1	
C26	0693,336	CPCTR 33N DCPLR SMD 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C27	0693,336	CPCTR 33N DCPLR SMD 805	1	
C28	0693,336	CPCTR 33N DCPLR SMD 805	1	
C29	0647,001	CPCTR 10U ALEC 16V SMD	1	
C30	0693,336	CPCTR 33N DCPLR SMD 805	1	
C31	0690,101	CPCTR 100P CML 2% 0805	1	
C32	0690,680	CPCTR 68P CML 2% 0805	1	
C33	0693,336	CPCTR 33N DCPLR SMD 805	1	
C34	0690,101	CPCTR 100P CML 2% 0805	1	
C35	0690,101	CPCTR 100P CML 2% 0805	1	
C36	0691,102	CPCTR 1N CML 10% 0805	1	
C37	0693,336	CPCTR 33N DCPLR SMD 805	1	
C38	0693,336	CPCTR 33N DCPLR SMD 805	1	
C39	0691,102	CPCTR 1N CML 10% 0805	1	
C40	0690,101	CPCTR 100P CML 2% 0805	1	
C41	0690,101	CPCTR 100P CML 2% 0805	1	
C42	0691,102	CPCTR 1N CML 10% 0805	1	
C43	0691,102	CPCTR 1N CML 10% 0805	1	
C44	0693,336	CPCTR 33N DCPLR SMD 805	1	
C45	0691,102	CPCTR 1N CML 10% 0805	1	
C46	0693,336	CPCTR 33N DCPLR SMD 805	1	
C47	0693,336	CPCTR 33N DCPLR SMD 805	1	
C48	0693,336	CPCTR 33N DCPLR SMD 805	1	
C49	0691,102	CPCTR 1N CML 10% 0805	1	
C50	0691,102	CPCTR 1N CML 10% 0805	1	
C51	0691,102	CPCTR 1N CML 10% 0805	1	
C52	0693,336	CPCTR 33N DCPLR SMD 805	1	
C53	0647,001	CPCTR 10U ALEC 16V SMD	1	
C54	0690,101	CPCTR 100P CML 2% 0805	1	
C55	0690,101	CPCTR 100P CML 2% 0805	1	
C56	0690,101	CPCTR 100P CML 2% 0805	1	
C57	0690,101	CPCTR 100P CML 2% 0805	1	
C58	0690,101	CPCTR 100P CML 2% 0805	1	
C59	0647,001	CPCTR 10U ALEC 16V SMD	1	
C60	0647,001	CPCTR 10U ALEC 16V SMD	1	
C61	0647,002	CPCTR 47U ALEC 16V SMD	1	
C62	0693,336	CPCTR 33N DCPLR SMD 805	1	
C63	0693,336	CPCTR 33N DCPLR SMD 805	1	
C64	0681,101	CPCTR 10U TANT SMD 16V	1	
C65	0635,230	CPCTR 220U ALEC 16V RAD	1	
C66	0693,336	CPCTR 33N DCPLR SMD 805	1	
C67	0693,336	CPCTR 33N DCPLR SMD 805	1	
C68				NOT FITTED
C69	0690,101	CPCTR 100P CML 2% 0805	1	
C70	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C71	0693,336	CPCTR 33N DCPLR SMD 805	1	
C72	0693,336	CPCTR 33N DCPLR SMD 805	1	
C73	0635,230	CPCTR 220U ALEC 16V RAD	1	
C74	0647,002	CPCTR 47U ALEC 16V SMD	1	
C75	0693,336	CPCTR 33N DCPLR SMD 805	1	
C76				NOT FITTED
C77	0693,336	CPCTR 33N DCPLR SMD 805	1	
C78	0693,336	CPCTR 33N DCPLR SMD 805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C79	0647,002	CPCTR 47U ALEC 16V SMD	1	
C80	0693,107	CPCTR 100N DCPLR SMD 805	1	
C81	0693,107	CPCTR 100N DCPLR SMD 805	1	
C82	0693,336	CPCTR 33N DCPLR SMD 805	1	
C83	0693,336	CPCTR 33N DCPLR SMD 805	1	
C84	0693,336	CPCTR 33N DCPLR SMD 805	1	
C85	0693,336	CPCTR 33N DCPLR SMD 805	1	
C86	0647,001	CPCTR 10U ALEC 16V SMD	1	
C87	0647,002	CPCTR 47U ALEC 16V SMD	1	
C88	0681,100	CPCTR 47U TANT SMD 10V	1	
C89				NOT FITTED
C90	0647,001	CPCTR 10U ALEC 16V SMD	1	
C91	0647,001	CPCTR 10U ALEC 16V SMD	1	
C92	0690,220	CPCTR 22P CML 2% 0805	1	
C93	0647,002	CPCTR 47U ALEC 16V SMD	1	
C94	0693,336	CPCTR 33N DCPLR SMD 805	1	
C95	0690,220	CPCTR 22P CML 2% 0805	1	
C96	0693,336	CPCTR 33N DCPLR SMD 805	1	
C97	0693,336	CPCTR 33N DCPLR SMD 805	1	
C98	0693,336	CPCTR 33N DCPLR SMD 805	1	
C99	0693,336	CPCTR 33N DCPLR SMD 805	1	
C100	0690,220	CPCTR 22P CML 2% 0805	1	
C101	0693,107	CPCTR 100N DCPLR SMD 805	1	
C102	0693,336	CPCTR 33N DCPLR SMD 805	1	
C103	0690,220	CPCTR 22P CML 2% 0805	1	
C104	0693,336	CPCTR 33N DCPLR SMD 805	1	
C105	0691,102	CPCTR 1N CML 10% 0805	1	
C106	0693,107	CPCTR 100N DCPLR SMD 805	1	
C107	0693,336	CPCTR 33N DCPLR SMD 805	1	
C108	0693,336	CPCTR 33N DCPLR SMD 805	1	
C109	0693,336	CPCTR 33N DCPLR SMD 805	1	
C110	0693,336	CPCTR 33N DCPLR SMD 805	1	
C111	0691,102	CPCTR 1N CML 10% 0805	1	
C112	0693,107	CPCTR 100N DCPLR SMD 805	1	
C113	0693,336	CPCTR 33N DCPLR SMD 805	1	
C114	0691,102	CPCTR 1N CML 10% 0805	1	
C115	0693,336	CPCTR 33N DCPLR SMD 805	1	
C116	0647,002	CPCTR 47U ALEC 16V SMD	1	
C117	0693,336	CPCTR 33N DCPLR SMD 805	1	
C118	0693,336	CPCTR 33N DCPLR SMD 805	1	
C119	0691,471	CPCTR 470P CML 10% 0805	1	
C120	0693,336	CPCTR 33N DCPLR SMD 805	1	
C121	0693,336	CPCTR 33N DCPLR SMD 805	1	
C122	0647,000	CPCTR 4U7 ALEC 25V SMD	1	
C123	0647,002	CPCTR 47U ALEC 16V SMD	1	
C124	0693,336	CPCTR 33N DCPLR SMD 805	1	
C125	0692,103	CPCTR 10N CML 20% 0805	1	
C126	0693,336	CPCTR 33N DCPLR SMD 805	1	
C127	0691,471	CPCTR 470P CML 10% 0805	1	
C128	0691,333	CPCTR 33N CML 10% 0805	1	
C129	0693,107	CPCTR 100N DCPLR SMD 805	1	
C130	0693,107	CPCTR 100N DCPLR SMD 805	1	
C131	0691,102	CPCTR 1N CML 10% 0805	1	
C132	0693,107	CPCTR 100N DCPLR SMD 805	1	
C133	0647,001	CPCTR 10U ALEC 16V SMD	1	
C134	0647,005	CPCTR 1U0 ALEC 50V SMD	1	
C135	0693,336	CPCTR 33N DCPLR SMD 805	1	
C136	0647,002	CPCTR 47U ALEC 16V SMD	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
C137				NOT FITTED
C138	0690,101	CPCTR 100P CML 2% 0805	1	
C139	0647,002	CPCTR 47U ALEC 16V SMD	1	
C140	0693,336	CPCTR 33N DCPLR SMD 805	1	
C141	0690,056	CPCTR 5P6 CML SMD 10% 805	1	
C142	0693,336	CPCTR 33N DCPLR SMD 805	1	
C143	0693,336	CPCTR 33N DCPLR SMD 805	1	
C144	0693,336	CPCTR 33N DCPLR SMD 805	1	
C145	0647,001	CPCTR 10U ALEC 16V SMD	1	
C146	0691,102	CPCTR 1N CML 10% 0805	1	
C147	0691,332	CPCTR 3N3 CML 10% 0805	1	
C148	0693,336	CPCTR 33N DCPLR SMD 805	1	
C149	0691,333	CPCTR 33N CML 10% 0805	1	
C150	0691,332	CPCTR 3N3 CML 10% 0805	1	
C151	0691,332	CPCTR 3N3 CML 10% 0805	1	
C152	0635,230	CPCTR 220U ALEC 16V RAD	1	
C153	0691,332	CPCTR 3N3 CML 10% 0805	1	
C154	0693,336	CPCTR 33N DCPLR SMD 805	1	
C155	0692,473	CPCTR 47N CML 20% 0805	1	
C156	0691,102	CPCTR 1N CML 10% 0805	1	
C157	0691,102	CPCTR 1N CML 10% 0805	1	
C158	0691,102	CPCTR 1N CML 10% 0805	1	
C159	0691,333	CPCTR 33N CML 10% 0805	1	
C160	0692,473	CPCTR 47N CML 20% 0805	1	
C161	0635,230	CPCTR 220U ALEC 16V RAD	1	
C162	0635,230	CPCTR 220U ALEC 16V RAD	1	
C163	0691,153	CPCTR 15N CML 10% 0805	1	
C164	0647,001	CPCTR 10U ALEC 16V SMD	1	
C165	0692,473	CPCTR 47N CML 20% 0805	1	
C166	0692,473	CPCTR 47N CML 20% 0805	1	
C167	0692,473	CPCTR 47N CML 20% 0805	1	
C168	0642,103	CPCTR 100U ALEC 25V RAD	1	
C169	0691,682	CPCTR 6N8 CML 10% 0805	1	
C170	0691,682	CPCTR 6N8 CML 10% 0805	1	
C171	0691,153	CPCTR 15N CML 10% 0805	1	
C172	0647,002	CPCTR 47U ALEC 16V SMD	1	
C173	0692,473	CPCTR 47N CML 20% 0805	1	
C174	0692,473	CPCTR 47N CML 20% 0805	1	
C175	0642,103	CPCTR 100U ALEC 25V RAD	1	
C176	0647,001	CPCTR 10U ALEC 16V SMD	1	
C177	0690,680	CPCTR 68P CML 2% 0805	1	
C178	0693,107	CPCTR 100N DCPLR SMD 805	1	
C500	0690,180	CPCTR 18P CML 2% 0805	1	
D1	0796,000	DIODE SI BAS16 SOT23	1	
D2	0796,000	DIODE SI BAS16 SOT23	1	
D3	0796,002	DIODE SI SB 0A1/20V SOT23	1	
D4	0796,000	DIODE SI BAS16 SOT23	1	
D5	0796,001	DIODE SI BAV99 SOT23	1	
D6	0796,000	DIODE SI BAS16 SOT23	1	
D7	0796,000	DIODE SI BAS16 SOT23	1	
D8	0796,000	DIODE SI BAS16 SOT23	1	
D9	0796,001	DIODE SI BAV99 SOT23	1	
D10	0796,000	DIODE SI BAS16 SOT23	1	
D11	0796,001	DIODE SI BAV99 SOT23	1	
FS1	0815,501	FUSE 2A F 63VAC SMD	1	
FS2	0815,500	FUSE 800MA F 63VAC SMD	1	
IC1	0759,574	IC 74ACT574 CMOS 20P SOIC	1	
IC2	0759,574	IC 74ACT574 CMOS 20P SOIC	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
IC3	0735,488	IC 1488 RS232 DRVR 14SOIC	1	
IC4	0758,999	IC 74AC04 VCO 14P SOIC	1	
IC5	0701,665	IC 37C665 UPCNTLR 100QFP	1	
IC6	0759,574	IC 74ACT574 CMOS 20P SOIC	1	
IC7	0735,489	IC 1489A RS232 RX 14SOIC	1	
IC8	0759,574	IC 74ACT574 CMOS 20P SOIC	1	
IC9	0759,004	IC 74ACT04 CMOS 14P SOIC	1	
IC10	0735,489	IC 1489A RS232 RX 14SOIC	1	
IC11	0759,032	IC 74ACT32 CMOS 14P SOIC	1	
IC12	0762,245	IC 74HCT245 CMOS 20P SOIC	1	
IC13	0297,030	IC IOMD REV.C 208QFP	1	
IC14				NOT FITTED
IC15				NOT FITTED
IC16	0762,245	IC 74HCT245 CMOS 20P SOIC	1	
IC17	0297,033	IC ETHERNET ID T092 0.1	1	
IC18	0762,014	IC 74HCT14 CMOS 14P SOIC	1	
IC19	0759,138	IC 74ACT138 CMOS 16P SOIC	1	
IC20	0708,584	IC 8583 RTC RAM 8P SOIC	1	
IC21	0759,139	IC 74ACT139 CMOS 16P SOIC	1	
IC22	0759,244	IC 74ACT244 CMOS 20P SOIC	1	
IC23	0759,573	IC 74ACT573 CMOS 20P SOIC	1	
IC24	0759,573	IC 74ACT573 CMOS 20P SOIC	1	
IC25	0764,241	IC 74LS241 TTL 20P SOIC	1	
IC26	0759,244	IC 74ACT244 CMOS 20P SOIC	1	
IC27	0297,034	IC RAS PAL (0760207)	1	
IC28	0759,573	IC 74ACT573 CMOS 20P SOIC	1	
IC29	0700,111	IC VIDC20 110MHZ 144P QFP	1	
IC30	0759,244	IC 74ACT244 CMOS 20P SOIC	1	
IC31	0759,573	IC 74ACT573 CMOS 20P SOIC	1	
IC32	0758,999	IC 74AC04 VCO 14P SOIC	1	
IC33	0759,244	IC 74ACT244 CMOS 20P SOIC	1	
IC34	0761,004	IC 74HC04 CMOS 14P SOIC	1	
IC35	0771,324	IC LM324 QUAD OP AMP SOIC	1	
IC36	0771,386	IC LM386 AUDIO AMP 8PSOIC	1	
L1	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L2	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L3	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L4	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L5	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L6	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L7	0860,504	CHOKE RF 2U2H 10% SMD1210	1	
L8	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L9	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L10	0860,505	CHOKE RF 33UH 10% SMD1210	1	
L11	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L12	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L13	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
LK1				NOT FITTED
LK2				NOT FITTED
LK3				NOT FITTED
LK4	0800,450	CONR 6W WAFR 0.1" ST PCB	1	
LK5	0800,051	CONR 3W WAFR 0.1" ST PCB	1	
LK6				NOT FITTED
LK7				NOT FITTED
LK8	0800,880	CONR 6W WAFR 2ROW 0.1"P	1	
LK9				NOT FITTED
LK10				NOT FITTED
LK11	0800,458	CONR 2W WAFR 0.1" ST LK	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
LK12	0800,459	CONR 4W WAFR 0.1" ST LK	1	
LK13	0800,883	CONR 10W WAFR 2ROW 0.1"	1	
LK14	0800,056	CONR 4W WAFR 0.1" ST PCB	1	
PL1	0800,298	CONRD 9WPLG RA PCB+RFI+L	1	
PL2	0803,102	CONR 34W BOX IDC LP ST	1	
PL3	0803,103	CONR 40W BOX IDC LP ST	1	
PL4	0803,305	CONR 6W PLG PCB DCPWR	1	
PL5	0804,016	CONR 16W WAFR 2ROW 2MM ST	1	
Q1	0784,859	TRANS BC859C PNP SOT23	1	
Q2	0784,859	TRANS BC859C PNP SOT23	1	
Q3	0784,849	TRANS BC849C NPN SOT23	1	
Q4	0778,207	VOLT REG 78L05 5V 8P SOIC	1	
Q5	0784,849	TRANS BC849C NPN SOT23	1	
Q6	0784,849	TRANS BC849C NPN SOT23	1	
R1				NOT FITTED
R2				NOT FITTED
R3				NOT FITTED
R4	0523,000	RES ZERO-R SMD 0W10 0805	1	
R5	0523,000	RES ZERO-R SMD 0W10 0805	1	
R6				NOT FITTED
R7				NOT FITTED
R8				NOT FITTED
R9	0523,000	RES ZERO-R SMD 0W10 0805	1	
R10	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R11	0523,331	RES 330R SMD 5% 0W10 0805	1	
R12	0523,470	RES 47R SMD 5% 0W10 0805	1	
R13	0523,820	RES 82R SMD 5% 0W10 0805	1	
R14	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R15	0523,680	RES 68R SMD 5% 0W10 0805	1	
R16				NOT FITTED
R17				NOT FITTED
R18				NOT FITTED
R19	0523,470	RES 47R SMD 5% 0W10 0805	1	
R20				NOT FITTED
R21				NOT FITTED
R22	0523,330	RES 33R SMD 5% 0W10 0805	1	
R23				NOT FITTED
R24				NOT FITTED
R25	0523,470	RES 47R SMD 5% 0W10 0805	1	
R26	0523,103	RES 10K SMD 5% 0W10 0805	1	
R27	0523,330	RES 33R SMD 5% 0W10 0805	1	
R28	0523,680	RES 68R SMD 5% 0W10 0805	1	
R29	0523,470	RES 47R SMD 5% 0W10 0805	1	
R30	0523,470	RES 47R SMD 5% 0W10 0805	1	
R31	0523,000	RES ZERO-R SMD 0W10 0805	1	
R32	0523,470	RES 47R SMD 5% 0W10 0805	1	
R33	0523,103	RES 10K SMD 5% 0W10 0805	1	
R34	0523,470	RES 47R SMD 5% 0W10 0805	1	
R35	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R36	0523,000	RES ZERO-R SMD 0W10 0805	1	
R37	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R38	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R39	0523,000	RES ZERO-R SMD 0W10 0805	1	
R40	0523,220	RES 22R SMD 5% 0W10 0805	1	
R41	0523,330	RES 33R SMD 5% 0W10 0805	1	
R42	0523,330	RES 33R SMD 5% 0W10 0805	1	
R43	0523,220	RES 22R SMD 5% 0W10 0805	1	
R44	0523,102	RES 1K0 SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R45	0523,000	RES ZERO-R SMD 0W10 0805	1	
R46	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R47	0523,680	RES 68R SMD 5% 0W10 0805	1	
R48	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R49	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R50	0523,330	RES 33R SMD 5% 0W10 0805	1	
R51				NOT FITTED
R52	0523,680	RES 68R SMD 5% 0W10 0805	1	
R53	0523,470	RES 47R SMD 5% 0W10 0805	1	
R54	0523,330	RES 33R SMD 5% 0W10 0805	1	
R55	0523,220	RES 22R SMD 5% 0W10 0805	1	
R56	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R57	0523,103	RES 10K SMD 5% 0W10 0805	1	
R58	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R59	0523,680	RES 68R SMD 5% 0W10 0805	1	
R60	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R61	0523,220	RES 22R SMD 5% 0W10 0805	1	
R62	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R63	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R64	0523,470	RES 47R SMD 5% 0W10 0805	1	
R65	0523,330	RES 33R SMD 5% 0W10 0805	1	
R66	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R67	0523,220	RES 22R SMD 5% 0W10 0805	1	
R68	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R69	0523,220	RES 22R SMD 5% 0W10 0805	1	
R70	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R71	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R72	0523,103	RES 10K SMD 5% 0W10 0805	1	
R73	0523,103	RES 10K SMD 5% 0W10 0805	1	
R74	0523,103	RES 10K SMD 5% 0W10 0805	1	
R75	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R76	0523,103	RES 10K SMD 5% 0W10 0805	1	
R77	0523,103	RES 10K SMD 5% 0W10 0805	1	
R78	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R79	0523,220	RES 22R SMD 5% 0W10 0805	1	
R80	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R81	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R82	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R83	0523,000	RES ZERO-R SMD 0W10 0805	1	
R84	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R85	0523,473	RES 47K SMD 5% 0W10 0805	1	
R86	0523,101	RES 100R SMD 5% 0W10 0805	1	
R87	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R88				NOT FITTED
R89	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R90	0523,470	RES 47R SMD 5% 0W10 0805	1	
R91				NOT FITTED
R92	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R93	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R94	0523,330	RES 33R SMD 5% 0W10 0805	1	
R95	0523,330	RES 33R SMD 5% 0W10 0805	1	
R96	0523,220	RES 22R SMD 5% 0W10 0805	1	
R97	0523,220	RES 22R SMD 5% 0W10 0805	1	
R98	0523,220	RES 22R SMD 5% 0W10 0805	1	
R99	0523,220	RES 22R SMD 5% 0W10 0805	1	
R100	0523,150	RES 15R SMD 5% 0W10 0805	1	
R101	0523,150	RES 15R SMD 5% 0W10 0805	1	
R102	0523,150	RES 15R SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R103	0523,150	RES 15R SMD 5% 0W10 0805	1	
R104	0523,220	RES 22R SMD 5% 0W10 0805	1	
R105	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R106	0523,220	RES 22R SMD 5% 0W10 0805	1	
R107	0523,330	RES 33R SMD 5% 0W10 0805	1	
R108	0523,220	RES 22R SMD 5% 0W10 0805	1	
R109	0523,220	RES 22R SMD 5% 0W10 0805	1	
R110	0523,220	RES 22R SMD 5% 0W10 0805	1	
R111	0523,150	RES 15R SMD 5% 0W10 0805	1	
R112	0523,150	RES 15R SMD 5% 0W10 0805	1	
R113	0523,220	RES 22R SMD 5% 0W10 0805	1	
R114	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R115	0523,150	RES 15R SMD 5% 0W10 0805	1	
R116	0523,150	RES 15R SMD 5% 0W10 0805	1	
R117	0523,150	RES 15R SMD 5% 0W10 0805	1	
R118				NOT FITTED
R119	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R120	0523,220	RES 22R SMD 5% 0W10 0805	1	
R121	0523,220	RES 22R SMD 5% 0W10 0805	1	
R122	0523,470	RES 47R SMD 5% 0W10 0805	1	
R123	0523,150	RES 15R SMD 5% 0W10 0805	1	
R124	0523,150	RES 15R SMD 5% 0W10 0805	1	
R125	0523,150	RES 15R SMD 5% 0W10 0805	1	
R126	0523,330	RES 33R SMD 5% 0W10 0805	1	
R127	0523,104	RES 100K SMD 5% 0W10 0805	1	
R128				NOT FITTED
R129	0523,220	RES 22R SMD 5% 0W10 0805	1	
R130	0523,181	RES 180R SMD 5% 0W10 0805	1	
R131	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R132	0523,470	RES 47R SMD 5% 0W10 0805	1	
R133	0523,470	RES 47R SMD 5% 0W10 0805	1	
R134	0523,470	RES 47R SMD 5% 0W10 0805	1	
R135	0523,680	RES 68R SMD 5% 0W10 0805	1	
R136	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R137	0523,331	RES 330R SMD 5% 0W10 0805	1	
R138	0523,470	RES 47R SMD 5% 0W10 0805	1	
R139	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R140	0523,470	RES 47R SMD 5% 0W10 0805	1	
R141	0523,122	RES 1K2 SMD 5% 0W10 0805	1	
R142				NOT FITTED
R143	0523,470	RES 47R SMD 5% 0W10 0805	1	
R144	0523,470	RES 47R SMD 5% 0W10 0805	1	
R145	0523,220	RES 22R SMD 5% 0W10 0805	1	
R146	0523,470	RES 47R SMD 5% 0W10 0805	1	
R147	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R148	0523,104	RES 100K SMD 5% 0W10 0805	1	
R149	0523,220	RES 22R SMD 5% 0W10 0805	1	
R150	0523,103	RES 10K SMD 5% 0W10 0805	1	
R151	0523,220	RES 22R SMD 5% 0W10 0805	1	
R152	0523,432	RES 4K3 SMD 5% 0W10 0805	1	
R153	0523,103	RES 10K SMD 5% 0W10 0805	1	
R154	0523,101	RES 100R SMD 5% 0W10 0805	1	
R155	0523,101	RES 100R SMD 5% 0W10 0805	1	
R156	0523,101	RES 100R SMD 5% 0W10 0805	1	
R157	0523,101	RES 100R SMD 5% 0W10 0805	1	
R158	0523,103	RES 10K SMD 5% 0W10 0805	1	
R159	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R160	0523,472	RES 4K7 SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R161	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R162	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R163	0523,393	RES 39K SMD 5% 0W10 0805	1	
R164	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R165	0523,103	RES 10K SMD 5% 0W10 0805	1	
R166	0523,220	RES 22R SMD 5% 0W10 0805	1	
R167	0523,331	RES 330R SMD 5% 0W10 0805	1	
R168	0523,220	RES 22R SMD 5% 0W10 0805	1	
R169	0523,220	RES 22R SMD 5% 0W10 0805	1	
R170				NOT FITTED
R171	0523,152	RES 1K5 SMD 5% 0W10 0805	1	
R172	0523,000	RES ZERO-R SMD 0W10 0805	1	
R173	0523,000	RES ZERO-R SMD 0W10 0805	1	
R174	0523,101	RES 100R SMD 5% 0W10 0805	1	
R175				NOT FITTED
R176	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R177	0523,330	RES 33R SMD 5% 0W10 0805	1	
R178				NOT FITTED
R179	0523,750	RES 75R SMD 5% 0W10 0805	1	
R180	0523,750	RES 75R SMD 5% 0W10 0805	1	
R181	0523,680	RES 68R SMD 5% 0W10 0805	1	
R182	0523,103	RES 10K SMD 5% 0W10 0805	1	
R183	0523,681	RES 680R SMD 5% 0W10 0805	1	
R184	0523,104	RES 100K SMD 5% 0W10 0805	1	
R185	0523,103	RES 10K SMD 5% 0W10 0805	1	
R186	0523,180	RES 18R SMD 5% 0W10 0805	1	
R187				NOT FITTED
R188	0523,273	RES 27K SMD 5% 0W10 0805	1	
R189	0523,750	RES 75R SMD 5% 0W10 0805	1	
R190	0523,331	RES 330R SMD 5% 0W10 0805	1	
R191	0523,103	RES 10K SMD 5% 0W10 0805	1	
R192	0523,680	RES 68R SMD 5% 0W10 0805	1	
R193	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R194	0523,153	RES 15K SMD 5% 0W10 0805	1	
R195	0521,102	RES 1K0 SMD 5% 0W25 1206	1	
R196	0523,332	RES 3K3 SMD 5% 0W10 0805	1	
R197	0523,680	RES 68R SMD 5% 0W10 0805	1	
R198	0523,471	RES 470R SMD 5% 0W10 0805	1	
R199	0523,392	RES 3K9 SMD 5% 0W10 0805	1	
R200	0523,223	RES 22K SMD 5% 0W10 0805	1	
R201	0523,101	RES 100R SMD 5% 0W10 0805	1	
R202				NOT FITTED
R203	0523,103	RES 10K SMD 5% 0W10 0805	1	
R204	0523,223	RES 22K SMD 5% 0W10 0805	1	
R205	0523,103	RES 10K SMD 5% 0W10 0805	1	
R206	0523,392	RES 3K9 SMD 5% 0W10 0805	1	
R207				NOT FITTED
R208	0523,103	RES 10K SMD 5% 0W10 0805	1	
R209	0523,103	RES 10K SMD 5% 0W10 0805	1	
R210	0523,223	RES 22K SMD 5% 0W10 0805	1	
R211	0523,223	RES 22K SMD 5% 0W10 0805	1	
R212	0523,181	RES 180R SMD 5% 0W10 0805	1	
R213	0523,820	RES 82R SMD 5% 0W10 0805	1	
R214	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R215	0523,103	RES 10K SMD 5% 0W10 0805	1	
R216	0523,103	RES 10K SMD 5% 0W10 0805	1	
R217	0523,102	RES 1K0 SMD 5% 0W10 0805	1	
R218	0523,682	RES 6K8 SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R219	0523,272	RES 2K7 SMD 5% 0W10 0805	1	
R220	0523,272	RES 2K7 SMD 5% 0W10 0805	1	
R221	0523,100	RES 10R SMD 5% 0W10 0805	1	
R222	0523,103	RES 10K SMD 5% 0W10 0805	1	
R223	0523,103	RES 10K SMD 5% 0W10 0805	1	
R224	0523,103	RES 10K SMD 5% 0W10 0805	1	
R225	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R226	0523,101	RES 100R SMD 5% 0W10 0805	1	
R227	0523,181	RES 180R SMD 5% 0W10 0805	1	
R228	0523,103	RES 10K SMD 5% 0W10 0805	1	
R229	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R230	0523,330	RES 33R SMD 5% 0W10 0805	1	
R231	0523,331	RES 330R SMD 5% 0W10 0805	1	
R232	0523,220	RES 22R SMD 5% 0W10 0805	1	
R233	0521,181	RES 180R SMD 5% 0W25 1206	1	
R234	0521,181	RES 180R SMD 5% 0W25 1206	1	
R235	0523,330	RES 33R SMD 5% 0W10 0805	1	
RP1	0576,470	RESNET 47RX8 5% 16P SOIC	1	
RP2	0576,470	RESNET 47RX8 5% 16P SOIC	1	
RP3	0576,470	RESNET 47RX8 5% 16P SOIC	1	
RP4	0576,330	RESNET 33RX8 5% 16P SOIC	1	
RP5	0576,330	RESNET 33RX8 5% 16P SOIC	1	
RP6	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP7	0577,104	RESNET 100KX15 5% 16PSOIC	1	
RP8	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP9	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP10	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP11	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP12	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP13	0576,680	RESNET 68RX8 5% 16P SOIC	1	
RP14	0577,104	RESNET 100KX15 5% 16PSOIC	1	
RP15	0577,104	RESNET 100KX15 5% 16PSOIC	1	
RP16	0576,680	RESNET 68RX8 5% 16P SOIC	1	
SK1	0800,408	CONR 96W SKT ST ABC PCB	1	
SK2	0800,408	CONR 96W SKT ST ABC PCB	1	
SK3	0800,299	CONRD 25W SKT RAPCB+RFI+L	1	
SK4	0800,416	CONR 48W SKT ST ABC PCB C	1	
SK5	0800,925	CONR 9W SKT M/DIN RA RFI	1	
SK6	0800,322	CONR 72W SIMM SKT 40DEG	1	
SK7	0800,322	CONR 72W SIMM SKT 40DEG	1	
SK8	0800,923	SKT 6W MINDIN RA PCB RFI	1	
SK9	0800,324	CONR 136W DIMM SKT 0.05"	1	
SK10	0800,281	CONRD 15WSKT RA HD+RFI+L	1	
SK11	0800,323	CONR 132W CARD EDGE 0.05"	1	
SK12	0800,644	CONR 3,5MM RA PCB JKSKT	1	
SW1	0805,710	SW 1P MOM PTM P/B RA PCB	1	
X1	0820,641	XTAL OSC 64MHZ CMOS 8P SB	1	
X2	0820,244	XTAL OSC 24MHZ CMOS 8P SB	1	
X3	0821,327	XTAL 32.768KHZ CC 0.05P	1	
Z1	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	
Z2	0796,101	DIODE 4V7 ZNR 0W3 SOT23	1	

Risc PC 2W Backplane PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,101	BARE PCB	1	
2	0197,101/A	PCB ASSEMBLY DWG	1	Per Batch
3	0197,101/C	PCB CIRCUIT DIAGRAM	1	Per Batch
4				
5				
6				
7				
8				
9				
10				
11				
12	0884,039	RIVET POP 3/32"D FOR 64W	4	Use on SK1, SK2
	0884,036	RIVET PLST SNAP 4,5THK	4	Option
14				
15				
16				
17				
18	0902,014	LABEL PCB SERIAL No 40x10	1	
19				
20				
C1	0680,102	CPCTR 100N DCPLR AXA 25V	1	
C2	0680,002	CPCTR 33/47N DCPLR 0.2"	1	
C3	0680,002	CPCTR 33/47N DCPLR 0.2"	1	
C4	0680,102	CPCTR 100N DCPLR AXA 25V	1	
C5	0622,470	CPCTR 47U ALEC 16V AX	1	
C6	0622,470	CPCTR 47U ALEC 16V AX	1	
C7	0622,470	CPCTR 47U ALEC 16V AX	1	
D1	0794,148	DIODE SI 1N4148	1	
IC1	0750,139	IC 74AC139 CMOS 16/0.3"	1	
IC2	0750,138	IC 74AC138 CMOS 16/0.3"	1	
PCB1				NOT FITTED
PCB2				NOT FITTED
Q1	0779,002	VOLT REG 7905 -5V/1.5A	1	
R1	0502,680	RES 68R C/MF 5% 0W25	1	
R2	0502,680	RES 68R C/MF 5% 0W25	1	
R3	0502,680	RES 68R C/MF 5% 0W25	1	
R4	0502,680	RES 68R C/MF 5% 0W25	1	
R5	0502,680	RES 68R C/MF 5% 0W25	1	
R6	0502,680	RES 68R C/MF 5% 0W25	1	
R7	0502,473	RES 47K C/MF 5% 0W25	1	
SK1	0800,408	CONR 96W SKT ST ABC PCB	1	
	0800,417	CONR 96W SKT ST ABC P.F	1	Option
SK2	0800,408	CONR 96W SKT ST ABC PCB	1	
	0800,417	CONR 96W SKT ST ABC P.F	1	Option

Risc PC 4W Backplane PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,001	BARE PCB	1	
2	0197,001/A	PCB ASSEMBLY DW	1	Per Batch
3	0197,001/C	PCB CIRCUIT DIAGRAM	1	Per Batch
4				
5				
6				
7				
8				
9				
10				
11				
12	0884,039	RIVET POP 3/32"D FQR 64W	8	Use on SK1, SK2, SK3, SK4
	0884,036	RIVET PLST SNAP 4,5THK	8	Option
14				
15				
16				
17				
18	0902,014	LABEL PCB SERIAL No 40x10	1	
19				
20				
C1	0622,470	CPCTR 47U ALEC 16V AX	1	
C2	0622,470	CPCTR 47U ALEC 16V AX	1	
C3	0622,470	CPCTR 47U ALEC 16V AX	1	
C4	0680,002	CPCTR 33/47N DCPLR 0.2"	1	
C5	0680,102	CPCTR 100N DCPLR AXA 25V	1	
C6	0680,002	CPCTR 33/47N DCPLR 0.2"	1	
C7	0680,102	CPCTR 100N DCPLR AXA 25V	1	
D1	0794,148	DIODE SI 1N4148	1	
IC1	0750,139	IC 74AC139 CMOS 16/0.3"	1	
IC2	0750,138	IC 74AC138 CMOS 16/0.3"	1	
PCB1				NOT FITTED
PCB2				NOT FITTED
Q1	0779,002	VOLT REG 7905 -5V/1.5A	1	
R1	0502,680	RES 68R C/MF 5% 0W25	1	
R2	0502,680	RES 68R C/MF 5% 0W25	1	
R3	0502,680	RES 68R C/MF 5% 0W25	1	
R4	0502,680	RES 68R C/MF 5% 0W25	1	
R5	0502,680	RES 68R C/MF 5% 0W25	1	
R6	0502,680	RES 68R C/MF 5% 0W25	1	
R7	0502,680	RES 68R C/MF 5% 0W25	1	
R8	0502,680	RES 68R C/MF 5% 0W25	1	
R9	0502,680	RES 68R C/MF 5% 0W25	1	
R10	0502,680	RES 68R C/MF 5% 0W25	1	
R11	0502,680	RES 68R C/MF 5% 0W25	1	
R12	0502,680	RES 68R C/MF 5% 0W25	1	
R13	0502,473	RES 47K C/MF 5% 0W25	1	
SK1	0800,417	CONR 96W SKT ST ABC P.F	1	
SK2	0800,417	CONR 96W SKT ST ABC P.F	1	
SK3	0800,417	CONR 96W SKT ST ABC P.F	1	
SK4	0800,417	CONR 96W SKT ST ABC P.F	1	

Risc PC 2MB HD final assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0097,625/A	Final Assy Drg	1	Per Batch
2				
3				
4				
5				
6	0197,000	Risc PC Main PCB	1	
7				
8		NOT fitted on this assy.		
9				
10				
11	0297,025	Moulding - Hinge Clip	1	
12				
13				
14				
15	0297,065	Clip Hard Disc Retaining	1	
16	0297,066	Clip Floppy Disc Drive	1	
17	0297,067	Button - On/Off	1	
18	0297,069	Fixing Front (Short)	2	
19				
20				
21				
22				
23	0297,079	Door Pivot Lever	1	
24	0297,077	Fixing Rear (Short)	2	
25				
26	0297,084	EMC - Base Moulding	1	
27	0297,085	EMC - Middle Moulding	1	
28	0297,086	EMC - Lid Moulding	1	
29				
30	0297,093	Gasket Rear Exp. Aperture	2	
31	0197,094	Cable Ribbon Floppy Disc	1	
32	0197,095	Cable Ribbon Hard Disc	1	
33	0197,096	Cable Assy 40mm Speaker	1	
34	0197,097	Cable Amber/Green LED's	1	
35	0297,098	Plate Network Blank	1	
36				
37				
38				
39	0197,101	Risc PC 2W Backplane PCB	1	Use on Item 6
40	0497,105	Desktop Blank (Screened)	1	
41	0197,112	Risc PC 70W (220/240V) PSU	1	
42				
43				
44	0197,208	ARM610 Proc PCB	1	Use on Item 6
45				
46				
47	0297,521	Risc OS 3.5 (UK) RoM 1 (x16)	1	Use on Item 6
48	0297,522	Risc OS 3.5 (UK) RoM 2 (x16)	1	Use on Item 6
49				
50				
51	0497,115	Door (Screened)	1	
52				
53				
54				
55				
56				
57	0704,200	IC SIMM DRAM Module 2M	1	Use on Item 6

ITEM	PART No.	DESCRIPTION	QTY	Remarks
58	0880,101	Cbl Tie Lk 98mmL	1	Use on Item 41
59	0882,000	Scw M3x7+8D Wshr POSI SEM	1	Use on Item 41
60	0882,111	Scw M2.5x6 Pan HD POSI	4	Use on Item 30
61	0882,121	Scw M3x6 Pan HD POSI	3	Use on Items 6, 77
62	0882,992	Wshr ORing Rbr 7,01Dx1,0S	4	Use on Items 18, 24
63				
64	0884,500	Spring 25Lx6.2Dmm Extensn	1	Use on Items 23, 27
65				
66				
67	0890,010	Adh Matl Rubr Sealant	A/R	Use on Items 33, 34
	0940,008	Adh Hot Melt PLST UL94V-0		Option
69				
70	0890,016	Foot SA Rbr 21sqx8Hmm Gry	4	Use on Item 26
71				
72				
73				
74				
75	0297,567	210HD/NoVRAM (TBP 0912,030)	1	(Caution when handling)
76				
77	0912,032	Floppy Drive 1/2M 3.5"CG2	1	
78				
79	0940,010	Grease Plastic Lubricant	A/R	Use on Items 23, 51
80				

Risc PC 5MB HD final assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0097,625/A	Final Assy Drg	1	Per Batch
2				
3				
4				
5				
6	0197,000	Risc PC Main PCB	1	
7				
8	0197,003	Risc PC VRAM (1M) PCB Assy	1	Use on Item 6
9				
10				
11	0297,025	Moulding - Hinge Clip	1	
12				
13				
14				
15	0297,065	Clip Hard Disc Retaining	1	
16	0297,066	Clip Floppy Disc Drive	1	
17	0297,067	Button - On/Off	1	
18	0297,069	Fixing Front (Short)	2	
19				
20				
21				
22				
23	0297,079	Door Pivot Lever	1	
24	0297,077	Fixing Rear (Short)	2	
25				
26	0297,084	EMC - Base Moulding	1	
27	0297,085	EMC - Middle Moulding	1	
28	0297,086	EMC - Lid Moulding	1	
29				
30	0297,093	Gasket Rear Exp. Aperture	2	
31	0197,094	Cable Ribbon Floppy Disc	1	
32	0197,095	Cable Ribbon Hard Disc	1	
33	0197,096	Cable Assy 40mm Speaker	1	
34	0197,097	Cable Amber/Green LED's	1	
35	0297,098	Plate Network Blank	1	
36				
37				
38				
39	0197,101	Risc PC 2W Backplane PCB	1	Use on Item 6
40	0497,105	Desktop Blank (Screened)	1	
41	0197,112	Risc PC 70W (220/240V) PSU	1	
42				
43				
44	0197,208	ARM610 Proc PCB	1	Use on Item 6
45				
46				
47	0297,521	Risc OS 3.5 (UK) RoM 1 (x16)	1	Use on Item 6
48	0297,522	Risc OS 3.5 (UK) RoM 2 (x16)	1	Use on Item 6
49				
50				
51	0497,115	Door (Screened)	1	
52				
53				
54				
55				
56				
57	0704,201	IC SIMM DRAM Module 4M	1	Use on Item 6

ITEM	PART No.	DESCRIPTION	QTY	Remarks
58	0880,101	Cbl Tie Lk 98mmL	1	Use on Item 41
59	0882,000	Scw M3x7+8D Wshr POSI SEM	1	Use on Item 41
60	0882,111	Scw M2.5x6 Pan HD POSI	4	Use on Item 30
61	0882,121	Scw M3x6 Pan HD POSI	3	Use on Items 6, 77
62	0882,992	Wshr ORing Rbr 7,01Dx1,0S	4	Use on Items 18, 24
63				
64	0884,500	Spring 25Lx6.2Dmm Extensn	1	Use on Items 23, 27
65				
66				
67	0890,010	Adh Matl Rubr Sealant	A/R	Use on Items 33, 34
	0940,008	Adh Hot Melt PLST UL94V-0		Option
69				
70	0890,016	Foot SA Rbr 21sqx8Hmm Gry	4	Use on Item 26
71				
72				
73				
74				
75	0297,565	210HD/VRAM (TBP 0912,030)	1	(Caution when handling)
76				
77	0912,032	Floppy Drive 1/2M 3.5"CG2	1	
78				
79	0940,010	Grease Plastic Lubricant	A/R	Use on Items 23, 51
80				

Risc PC 9MB HD final assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0097,630/A	Final Assy Drg	1	Per Batch
2				
3				
4				
5				
6	0197,000	Risc PC Main PCB	1	
7				
8	0197,003	Risc PC VRAM (1M) PCB Assy	1	Use on Item 6
9				
10	0297,020	EMC - Middle Moulding II	1	
11	0297,025	Moulding - Hinge Clip	2	
12				
13				
14	0297,064	Moulding - Door	1	
15	0297,065	Clip Hard Disc Retaining	1	
16	0297,066	Clip Floppy Disc Drive	1	
17	0297,067	Button - On/Off	1	
18	0297,089	Fixing Front (Long)	2	
19				
20				
21	0297,072	Front - Blank	1	
22				
23	0297,079	Door Pivot Lever	2	
24	0297,090	Fixing Rear (Long)	2	
25				
26	0297,084	EMC - Base Moulding	1	
27	0297,085	EMC - Middle Moulding	1	
28	0297,086	EMC - Lid Moulding	1	
29				
30	0297,093	Gasket Rear Exp. Aperture	4	
31	0197,094	Cable Ribbon Floppy Disc	1	
32	0197,095	Cable Ribbon Hard Disc	1	
33	0197,096	Cable Assy 40mm Speaker	1	
34	0197,097	Cable Amber/Green LED's	1	
35	0297,098	Plate Network Blank	1	
36	0297,099	Gasket EMC (Steel)	1	
37				
38				
39	0197,001	Risc PC 4W Backplane PCB	1	Use on Item 6
40	0497,105	Desktop Blank (Screened)	1	
41	0197,012	Risc PC 103W (220/240V) PSU	1	
42				
43				
44	0197,208	ARM610 Proc PCB	1	Use on Item 6
45				
46				
47	0297,521	Risc OS 3.5 (UK) RoM 1 (x16)	1	Use on Item 6
48	0297,522	Risc OS 3.5 (UK) RoM 2 (x16)	1	Use on Item 6
49				
50				
51	0497,115	Door (Screened)	1	
52				
53				
54				
55				
56				
57	0704,202	IC SIMM DRAM Module 8M	1	Use on Item 6

ITEM	PART No.	DESCRIPTION	QTY	Remarks
58	0880,101	Cbl Tie Lk 98mmL	1	Use on Item 41
59	0882,000	Scw M3x7+8D Wshr POSI SEM	1	Use on Item 41
60	0882,111	Scw M2.5x6 Pan HD Posi	8	Use on Item 30
61	0882,121	Scw M3x6 Pan HD POSI	3	Use on Items 6, 77
62	0882,992	Wshr ORing Rbr 7,01Dx1,0S	4	Use on Items 18, 24
63				
64	0884,500	Spring 25Lx6.2Dmm Extensn	2	Use on Items 10, 23, 27
65				
66				
67	0890,010	Adh Matl Rubr Sealant	A/R	Use on Items 33, 34
	0940,008	Adh Hot Melt PLST UL94V-0		Option
69				
70	0890,016	Foot SA Rbr 21sqx8Hmm Gry	4	Use on Item 26
71				
72				
73				
74				
75	0297,566	420HD/VRAM (TBP 0912,031)	1	(Caution when handling)
76				
77	0912,032	Floppy Drive 1/2M 3.5"CG2	1	
78				
79	0940,010	Grease Plastic Lubricant	A/R	Use on Items 14, 23, 51
80				

Risc PC ARM610 PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,208	BARE PCB	1	
2	0197,208/A	PCB ASSEMBLY DRG	1	Per Batch
3	0197,208/C	PCB CIRCUIT DIAGRAM	1	Per Batch
4				
5				
6				
7				
8				
9				
10				
11				
12	0884,039	RIVET POP 3/32"D FOR 64W	2	Use on PL1
	0884,029	RIVET PLST SNAP 7,8THK		Option
14				
15				
16				
17				
18	0902,014	LABEL PCB SERIAL No 40x10	1	
19				
20				
C1	0621,470	CPCTR 47U ALEC 10V AX	1	
C2	0693,336	CPCTR 33N DCPLR SMD 805	1	
C3	0693,336	CPCTR 33N DCPLR SMD 805	1	
C4	0693,336	CPCTR 33N DCPLR SMD 805	1	
C5	0693,336	CPCTR 33N DCPLR SMD 805	1	
C6	0693,336	CPCTR 33N DCPLR SMD 805	1	
C7	0693,336	CPCTR 33N DCPLR SMD 805	1	
C8	0693,336	CPCTR 33N DCPLR SMD 805	1	
C9	0693,336	CPCTR 33N DCPLR SMD 805	1	
C10	0693,336	CPCTR 33N DCPLR SMD 805	1	
C11	0690,220	CPCTR 22P CML 2% 0805	1	
IC1	0700,113	IC ARM610 30MHZ 144P QFP	1	
IC2	0759,999	IC 74ACT74 CMOS SYM 14SO	1	
IC3	0759,008	IC 74ACT08 CMOS 14P SOIC	1	
PL1	0800,410	CONR 96W PLG RA ABC PCB	1	
R1	0523,101	RES 100R SMD 5% 0W10 0805	1	
R2	0523,103	RES 10K SMD 5% 0W10 0805	1	
R3	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R4	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R5	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R6	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R7	0523,330	RES 33R SMD 5% 0W10 0805	1	
R8	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R9	0523,472	RES 4K7 SMD 5% 0W10 0805	1	
R10	0523,330	RES 33R SMD 5% 0W10 0805	1	
R11	0523,330	RES 33R SMD 5% 0W10 0805	1	
R12	0523,330	RES 33R SMD 5% 0W10 0805	1	
R13	0523,330	RES 33R SMD 5% 0W10 0805	1	
R14	0523,330	RES 33R SMD 5% 0W10 0805	1	
R15	0523,330	RES 33R SMD 5% 0W10 0805	1	
R16	0523,330	RES 33R SMD 5% 0W10 0805	1	
R17	0523,330	RES 33R SMD 5% 0W10 0805	1	
R18	0523,330	RES 33R SMD 5% 0W10 0805	1	
R19	0523,330	RES 33R SMD 5% 0W10 0805	1	
R20	0523,330	RES 33R SMD 5% 0W10 0805	1	
R21	0523,330	RES 33R SMD 5% 0W10 0805	1	
R22	0523,330	RES 33R SMD 5% 0W10 0805	1	

ITEM	PART No.	DESCRIPTION	QTY	Remarks
R23	0523,330	RES 33R SMD 5% 0W10 0805	1	
R24	0523,330	RES 33R SMD 5% 0W10 0805	1	
R25	0523,330	RES 33R SMD 5% 0W10 0805	1	
R26	0523,330	RES 33R SMD 5% 0W10 0805	1	
R27	0523,330	RES 33R SMD 5% 0W10 0805	1	
R28	0523,330	RES 33R SMD 5% 0W10 0805	1	
R29	0523,330	RES 33R SMD 5% 0W10 0805	1	
R30	0523,330	RES 33R SMD 5% 0W10 0805	1	
R31	0523,330	RES 33R SMD 5% 0W10 0805	1	
R32	0523,330	RES 33R SMD 5% 0W10 0805	1	
R33	0523,330	RES 33R SMD 5% 0W10 0805	1	
R34	0523,330	RES 33R SMD 5% 0W10 0805	1	
R35	0523,330	RES 33R SMD 5% 0W10 0805	1	
R36	0523,330	RES 33R SMD 5% 0W10 0805	1	
R37	0523,330	RES 33R SMD 5% 0W10 0805	1	
R38	0523,330	RES 33R SMD 5% 0W10 0805	1	
R39	0523,330	RES 33R SMD 5% 0W10 0805	1	
R40	0523,330	RES 33R SMD 5% 0W10 0805	1	
R41	0523,330	RES 33R SMD 5% 0W10 0805	1	
X1	0820,601	XTAL OSC 60MHZ CMOS 8P	1	

Risc PC VRAM 1MB PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,003	BARE PCB	1	
2	0197,003/A	PCB ASSEMBLY DRG	1	Per Batch
3	0197,003/C	PCB CIRCUIT DIAGRAM	1	Per Batch
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18	0902,014	LABEL PCB SERIAL No 40x10	1	
19				
20				
C1	0693,107	CPCTR 100N DCPLR SMD 805	1	
C2	0693,107	CPCTR 100N DCPLR SMD 805	1	
C3	0693,107	CPCTR 100N DCPLR SMD 805	1	
C4	0693,107	CPCTR 100N DCPLR SMD 805	1	
C5				NOT FITTED
C6				NOT FITTED
C7				NOT FITTED
C8				NOT FITTED
C9	0647,002	CPCTR 47U ALEC 16V SMD	1	
C10	0647,002	CPCTR 47U ALEC 16V SMD	1	
C11	0647,002	CPCTR 47U ALEC 16V SMD	1	
C12	0647,002	CPCTR 47U ALEC 16V SMD	1	
C13				NOT FITTED
C14				NOT FITTED
C15				NOT FITTED
C16				NOT FITTED
IC1	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC2	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC3	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC4	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC21				NOT FITTED
IC22				NOT FITTED
IC23				NOT FITTED
IC24				NOT FITTED
L1	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L2	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L3	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L4	0860,503	IND CHK 1A 80R@100MHZ SMD	1	

Risc PC VRAM 2MB PCB assembly parts list

ITEM	PART No.	DESCRIPTION	QTY	Remarks
1	0297,003	BARE PCB	1	
2	0197,004/A	PCB ASSEMBLY DRG	1	Per Batch
3	0197,003/C	PCB CIRCUIT DIAGRAM	1	Per Batch
4				
5				
6				
7				
8	0497,049	VRAM (2M) PCB LABEL	1	
9				
10				
11				
12				
13				
14				
15				
16				
17				
18	0902,014	LABEL PCB SERIAL No 40x10	1	
19				
20				
C1	0693,107	CPCTR 100N DCPLR SMD 805	1	
C2	0693,107	CPCTR 100N DCPLR SMD 805	1	
C3	0693,107	CPCTR 100N DCPLR SMD 805	1	
C4	0693,107	CPCTR 100N DCPLR SMD 805	1	
C5	0693,107	CPCTR 100N DCPLR SMD 805	1	
C6	0693,107	CPCTR 100N DCPLR SMD 805	1	
C7	0693,107	CPCTR 100N DCPLR SMD 805	1	
C8	0693,107	CPCTR 100N DCPLR SMD 805	1	
C9	0647,002	CPCTR 47U ALEC 16V SMD	1	
C10	0647,002	CPCTR 47U ALEC 16V SMD	1	
C11	0647,002	CPCTR 47U ALEC 16V SMD	1	
C12	0647,002	CPCTR 47U ALEC 16V SMD	1	
C13	0693,107	CPCTR 100N DCPLR SMD 805	1	
C14	0693,107	CPCTR 100N DCPLR SMD 805	1	
C15	0693,107	CPCTR 100N DCPLR SMD 805	1	
C16	0693,107	CPCTR 100N DCPLR SMD 805	1	
IC1	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC2	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC3	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC4	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC21	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC22	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC23	0704,300	IC VRAM 256KX8 70NS TSOP	1	
IC24	0704,300	IC VRAM 256KX8 70NS TSOP	1	
L1	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L2	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L3	0860,503	IND CHK 1A 80R@100MHZ SMD	1	
L4	0860,503	IND CHK 1A 80R@100MHZ SMD	1	

Appendix A – Power On Self Test

A Power On Self Test (POST) is always carried out by the Risc PC immediately after power on. The POST code in the RISC OS 3.5 ROMs is Release 2.04 and is the version described here.

In a normal power-on test sequence, the screen colour is set to purple to indicate testing has started, whilst brief ROM and RAM tests are carried out. IOMD and VIDC are then initialised and tested. This phase passes quickly and may not easily be visible. However, some system failures may cause the machine to crash or halt during this phase, in which case no further activity will occur and this would indicate a major failure, most probably of the IO system.

The screen mode is next set depending on the state of the video ID[0] pin. Either to VGA if a VGA, SVGA or Multiscan monitor is connected which pulls the ID pin low, or to a TV style mode suitable for a simple 15kHz monitor (monitor_type 0, sync 0) if not. If a stable display is not shown on the monitor, it may indicate either a faulty monitor connection, a video system fault or some more fundamental fault which prevents the test software itself from running.

If the simple memory and IOMD / VIDC tests are passed, the screen colour is changed to blue and a more extensive memory test occurs followed by further brief tests on the video and sound system.

The screen colour now reverts to purple and the ARM processor ID is read. This test relies on good RAM, and will not be performed if a failure has already been detected. However, an unexpected failure could leave a purple screen displayed, indicating a major system fault.

The self-test is then complete and a green or red screen is displayed indicating a pass or fail condition. If there is a fault the screen is set to red whilst the floppy disk LED signals the fault code as given below.

However, if the machine passes self test the green screen will not normally be seen as the system will immediately start RISC OS. This is indicated by a black screen with a memory size message being displayed. Note that the various power on key combinations should be held until this message appears, as they will be ignored if released before the self-test sequence has completed.

The LED flashing sequence indicates the 8 digit hexadecimal fault code as 8 groups of 4 flashes, where a long flash indicates binary '1' and a short flash indicates binary '0'. Thus a ROM failure (fault code 00000219 on an ARM 610 machine) will be displayed as:

short	short	short	short	0
short	short	short	short	0
short	short	short	short	0
short	short	short	short	0
short	short	short	short	0
short	short	long	short	2
short	short	short	long	1
long	short	short	long	9

If a POST interface box is connected to the system, each individual test is displayed on the POST interface box LCD screen together with detailed pass/fail and other information. Each test is carried out slowly and the different test phases are clearly visible from the slowly changing screen colours. Finally an overall PASS/FAIL message is displayed on the LCD with the same result code as is signalled on the floppy LED. This will be either

PASS : xxxxxxxx
or FAIL : xxxxxxxx

where xxxxxxxx is a bitmap summarising the test results and other flags.

Fault and status codes

The fault and status codes are as follows:

Table 1.1: Status bits

Bit	Meaning
00000001	Self-test due to power-on
00000002	Self-test due to interface hardware
00000004	Self-test due to test link
00000008	Long memory test performed
00000010	ARM ID read and is not ARM 2
00000020	Long memory test disabled by SRAM flag
00000040	Integrated I/O controller fitted
00000080	VRAM present
00000100	CMOS RAM checksum error

Table 1.2: Fault bits

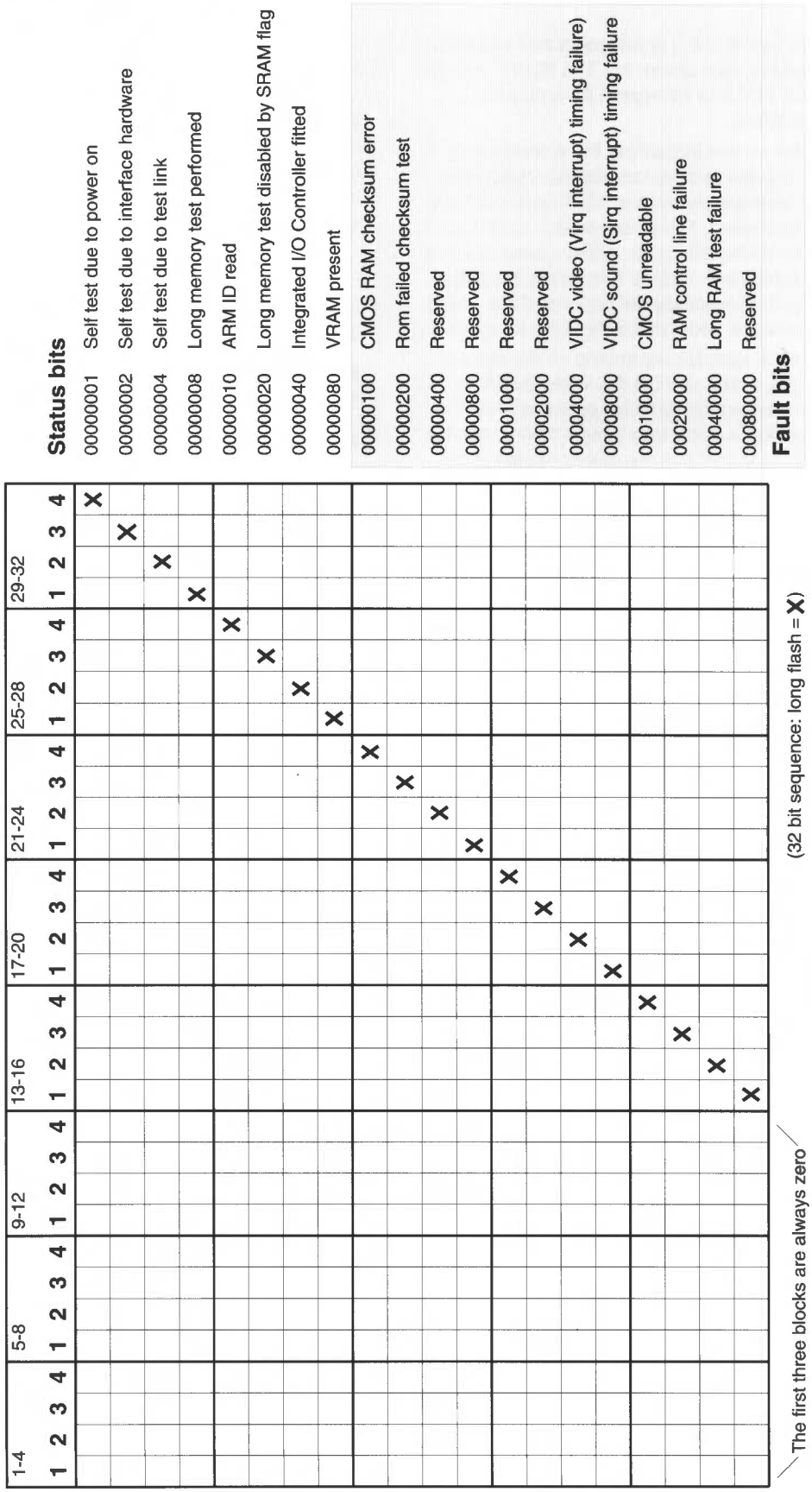
Bit	Meaning
00000200	ROM failed checksum test
00001000	IOC register test failed [V1.45]
00004000	VIDC (Virq interrupt) timing failed
00008000	Sound (Sirq interrupt) timing failed
00010000	CMOS unreadable [V1.43]
00020000	Ram control line failure
00040000	Long RAM test failure

Only bits 9 to 31 indicate faults. If a POST box is fitted any of the bits 0 to 7 may be set and the resulting code displayed along with the PASS message and a green screen. Bit patterns not defined above may be assigned to future versions of the test software.

If bit 7 of byte &BC in CMOS RAM is set the POST software will not perform the long memory test to avoid repeated long power on delays for when large memory configurations are used (i.e. above 64 MB). However, this also disables the VIDC tests (due to backwards compatibility with earlier versions of the POST software) and so should be avoided.

The table shown in *Figure 1.1* overleaf allows the fault and status codes to be read off from the relevant LED sequence.

Figure 1.1: Power on self test diagnosis

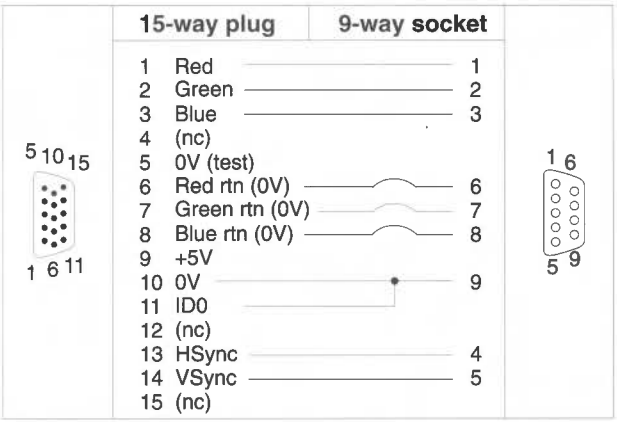


Appendix B – Monitor adaptor cables

This appendix describes how to make adaptor cables for monitors not supplied with a 15-way VGA connector.

15-way to 9-way adaptor for separate sync monitors

The cable supplied with some Multiscan monitors is terminated at the computer end with a 9-way D-type plug. You need a standard 15-way plug to 9-way socket adaptor:

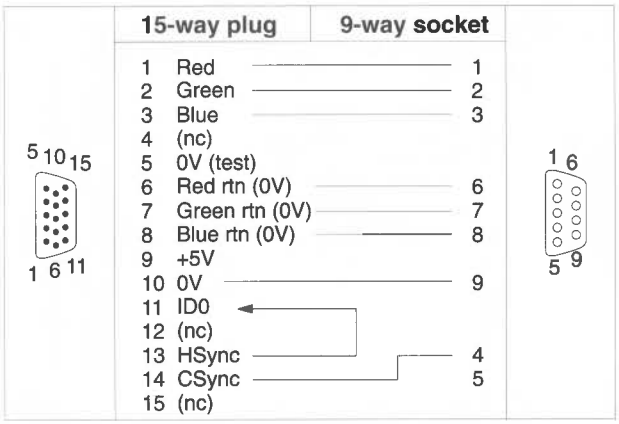


Note: The ID0 to 0V connection will make the computer generate separate sync signals.

Most Multiscan monitors are now being designed to be VGA-compatible and will work satisfactorily when driven with separate horizontal and vertical sync signals. The ID0 to 0V connection makes the computer generate separate sync signals.

15-way to 9-way adaptor for composite sync monitors

The cable supplied with some monitors is terminated at the computer end with a 9 pin D-type plug. You need a 15-way plug to 9-way socket adaptor:

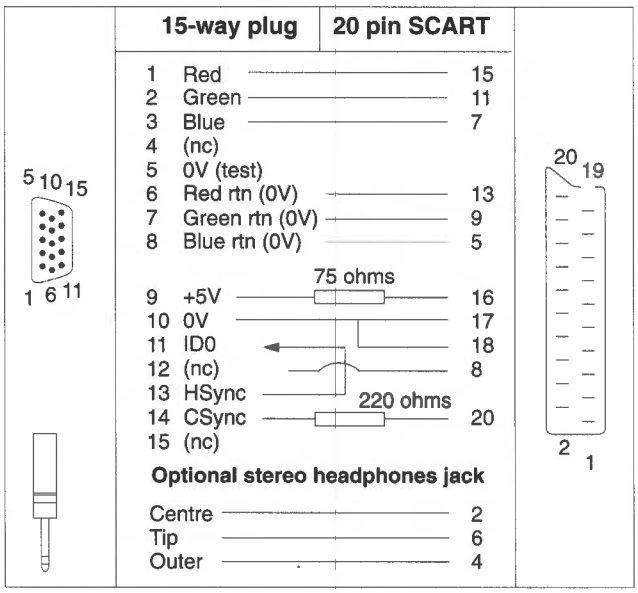


Note: HSync (pin 13) linked back into ID0 (pin 11) tells the computer that composite (rather than separate) sync is required, and that only modes compatible with a TV standard monitor can be displayed.

HSYNC to ID0 connection makes the computer generate a composite sync signal.

15-way to SCART input socket

You need to make this cable (if it's not supplied) for use with televisions and monitors using a SCART input socket:



Note 1: HSync (pin 13) linked back to ID0 (pin 11) tells the computer that composite (rather than vertical) sync is required, and that only modes compatible with a TV standard monitor can be displayed.

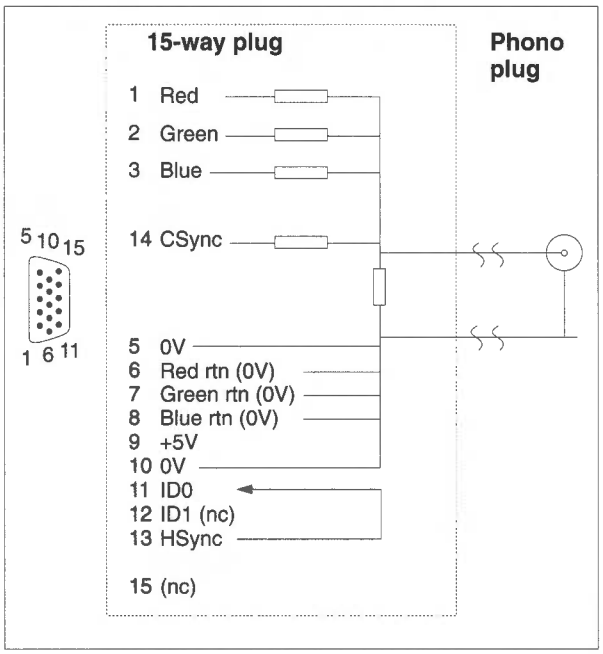
Note 2: On some TVs you might have to switch the TV manually into SCART mode (check how to do this in the TV's manual).

Connecting the stereo headphones jack will automatically cut off the sound to the computer's internal speaker.

Monochrome monitors

You need to make this cable to use with monochrome monitors which have a phono input socket. You need a 15-way plug to phono socket adaptor with resistors, to mix the separate red, green and blue signals into a composite monochrome signal (you can fit these components into a 15-way connector shell).

You need to make an adaptor cable that has a 15-way D-type plug on one end, and a phono plug on the other. The connections you need to make are as follows:



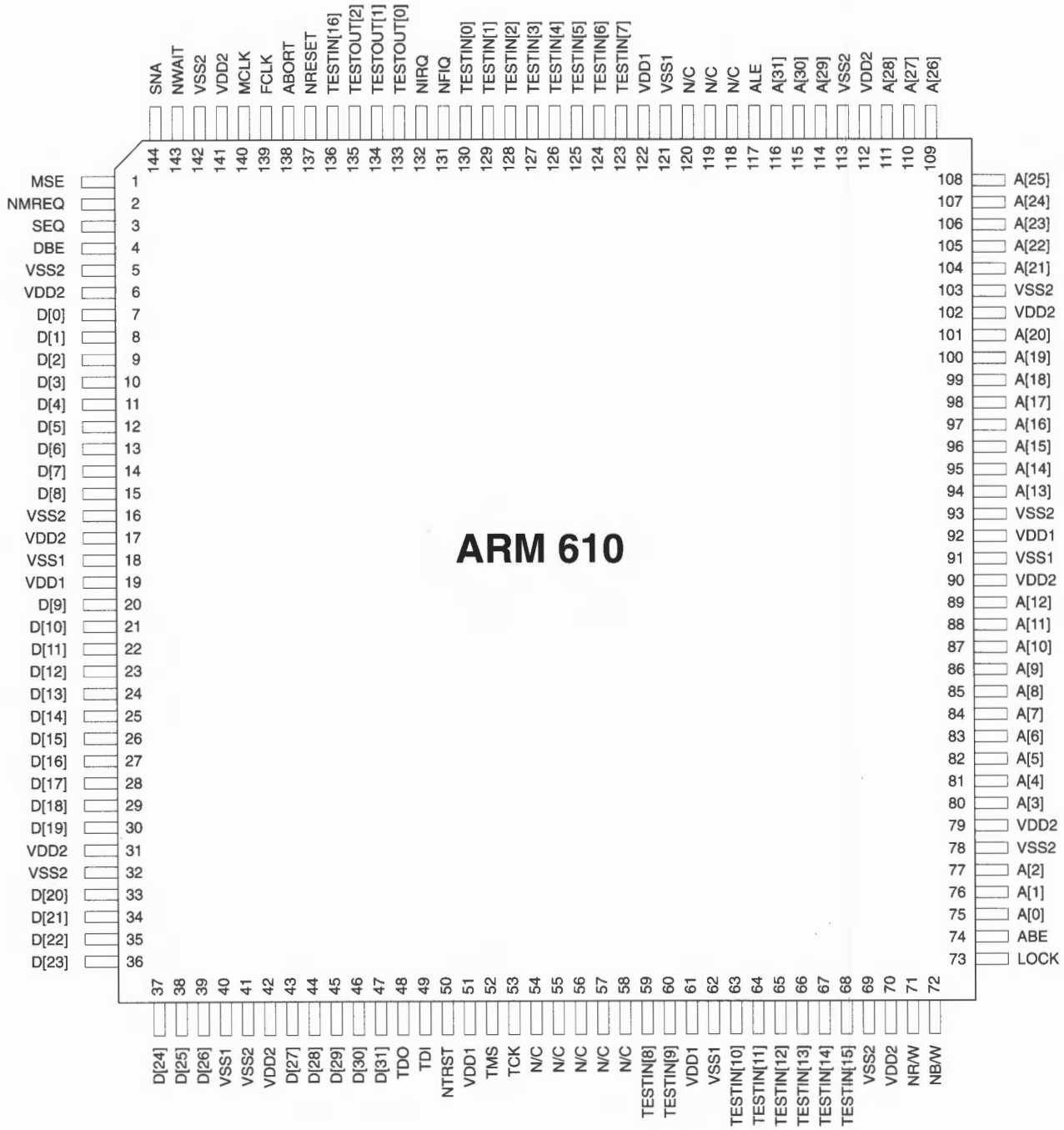
Appendix C – Engineering drawings

This appendix contains the following schematics:

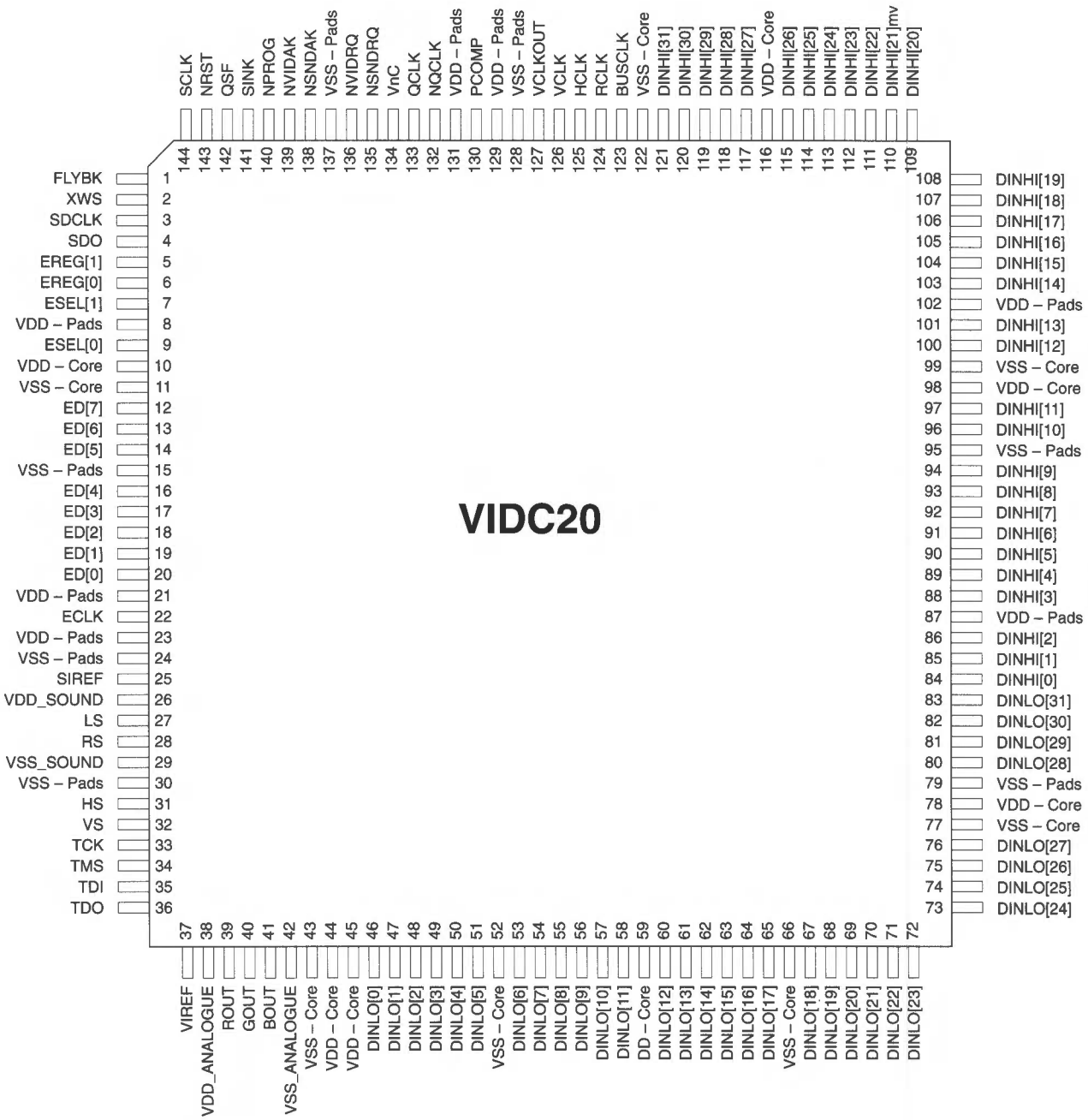
- Circuit schematics.
- PCB assembly drawings
- Final assembly drawings
- ARM610 PCB schematic
- ARM610 PCB assembly
- VRAM schematic
- VRAM PCB Assembly
- 2W Backplane schematics
- 2W Backplane PCB assembly
- 4W Backplane schematics
- 4W Backplane PCB assembly

Appendix D – System chipset pinouts

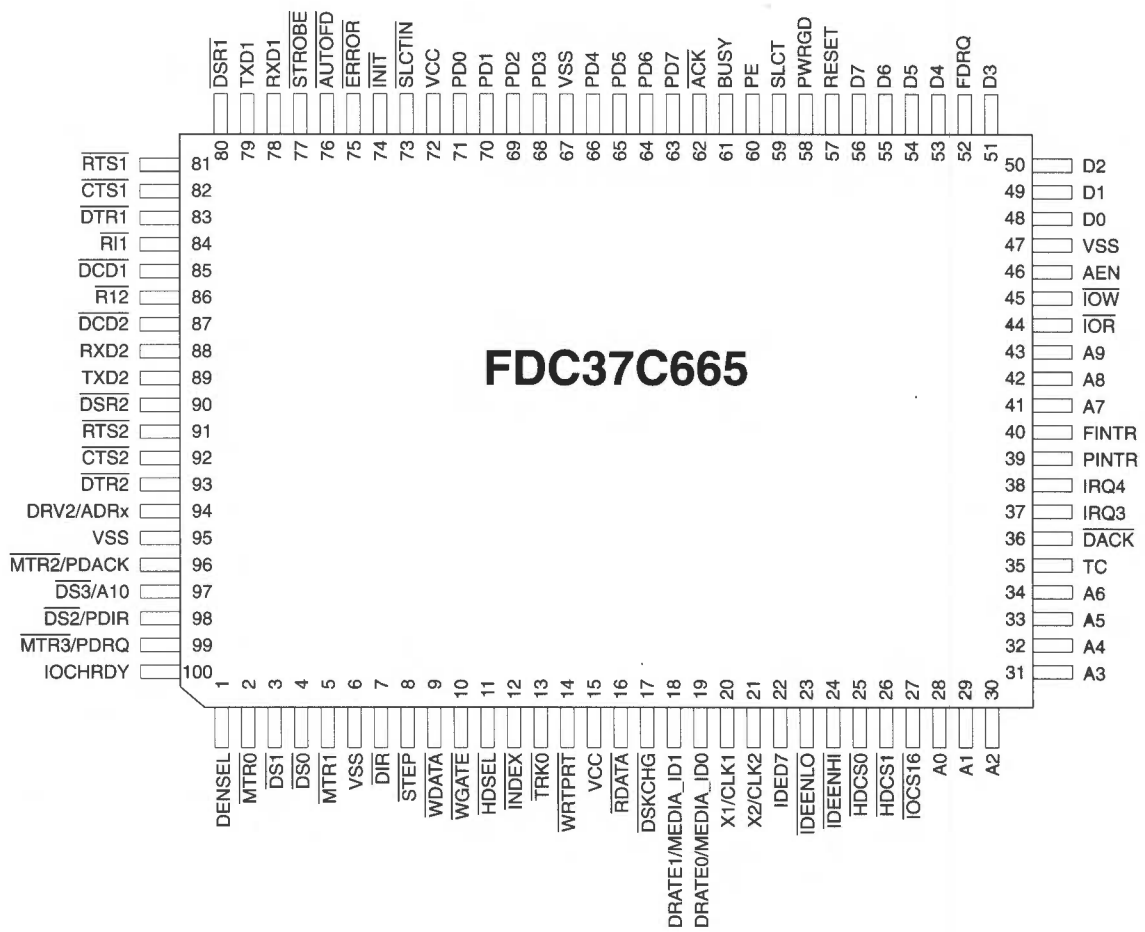
ARM610



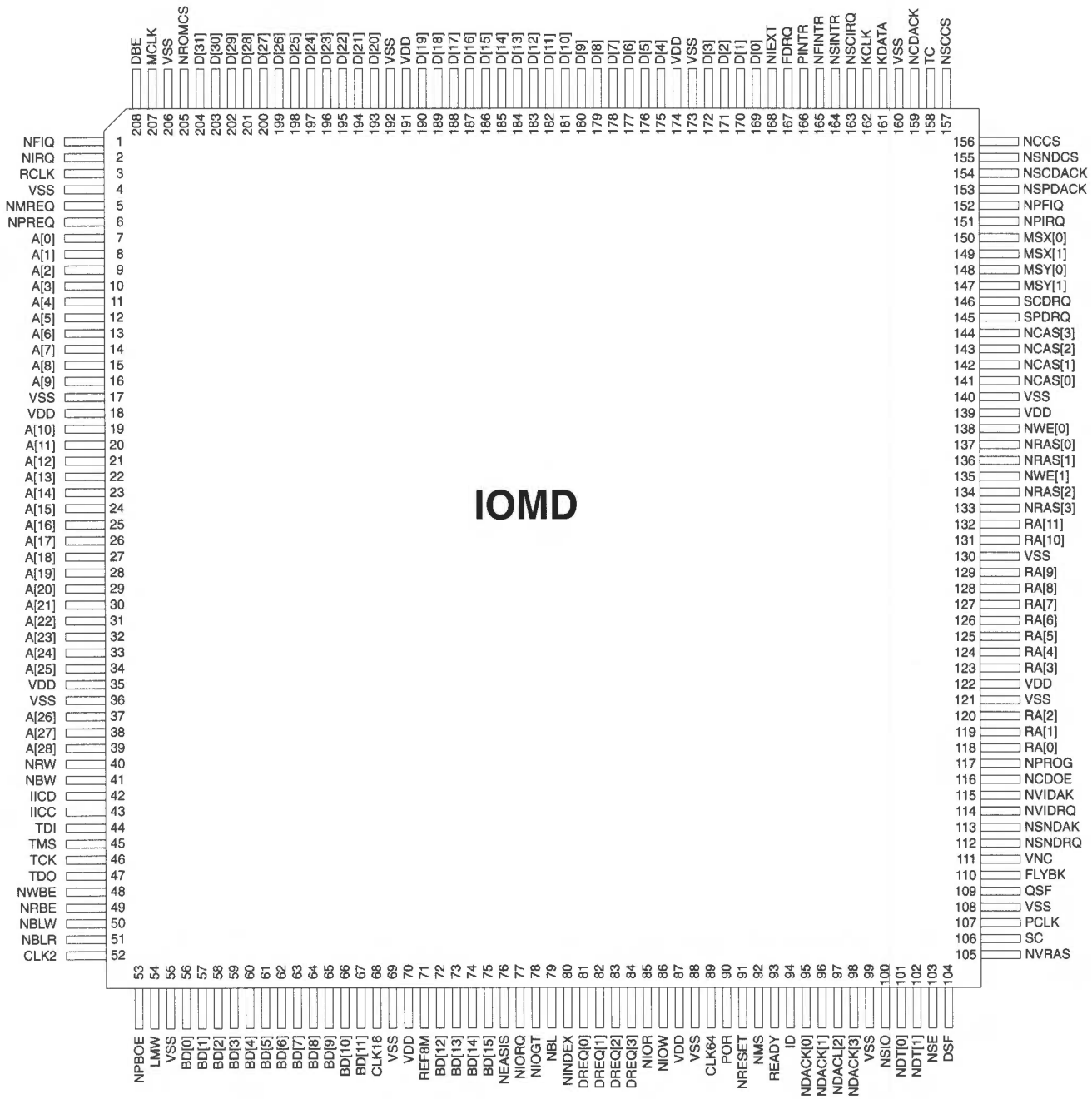
VIDC20


VIDC20
1 FLYBK
2 XWS
3 SDCLK
4 SDO
5 EREG[1]
6 EREG[0]
7 ESEL[1]
8 VDD – Pads
9 ESEL[0]
10 VDD – Core
11 VSS – Core
12 ED[7]
13 ED[6]
14 ED[5]
15 VSS – Pads
16 ED[4]
17 ED[3]
18 ED[2]
19 ED[1]
20 ED[0]
21 VDD – Pads
22 ECLK
23 VDD – Pads
24 VSS – Pads
25 SIREF
26 VDD_SOUND
27 LS
28 RS
29 VSS_SOUND
30 VSS – Pads
31 HS
32 VS
33 TCK
34 TMS
35 TDI
36 TDO
37 VIREF
38 VDD_ANALOGUE
39 ROUT
40 GOUT
41 BOUT
42 VSS_ANALOGUE
43 VSS – Core
44 VDD – Core
45 VDD – Core
46 DINLO[0]
47 DINLO[1]
48 DINLO[2]
49 DINLO[3]
50 DINLO[4]
51 DINLO[5]
52 VSS – Core
53 DINLO[6]
54 DINLO[7]
55 DINLO[8]
56 DINLO[9]
57 DINLO[10]
58 DINLO[11]
59 DD – Core
60 DINLO[12]
61 DINLO[13]
62 DINLO[14]
63 DINLO[15]
64 DINLO[16]
65 DINLO[17]
66 VSS – Core
67 DINLO[18]
68 DINLO[19]
69 DINLO[20]
70 DINLO[21]
71 DINLO[22]
72 DINLO[23]
73 DINLO[24]
74 DINLO[25]
75 DINLO[26]
76 DINLO[27]
77 VSS – Core
78 VDD – Core
79 VSS – Pads
80 DINLO[28]
81 DINLO[29]
82 DINLO[30]
83 DINLO[31]
84 DINHI[0]
85 DINHI[1]
86 DINHI[2]
87 VDD – Pads
88 DINHI[3]
89 DINHI[4]
90 DINHI[5]
91 DINHI[6]
92 DINHI[7]
93 DINHI[8]
94 DINHI[9]
95 VSS – Pads
96 DINHI[10]
97 DINHI[11]
98 VDD – Core
99 VSS – Core
100 DINHI[12]
101 DINHI[13]
102 VDD – Pads
103 DINHI[14]
104 DINHI[15]
105 DINHI[16]
106 DINHI[17]
107 DINHI[18]
108 DINHI[19]
109 DINHI[20]
110 DINHI[21]mv
111 DINHI[22]
112 DINHI[23]
113 DINHI[24]
114 DINHI[25]
115 DINHI[26]
116 VDD – Core
117 DINHI[27]
118 DINHI[28]
119 DINHI[29]
120 DINHI[30]
121 DINHI[31]
122 VSS – Core
123 BUSCLK
124 RCLK
125 HCLK
126 VCLK
127 VCLKOUT
128 VSS – Pads
129 VDD – Pads
130 PCOMP
131 VDD – Pads
132 NQCLK
133 QCLK
134 VnC
135 NSNDRQ
136 NVIDRQ
137 VSS – Pads
138 NSNDAK
139 NVIDAK
140 NPROG
141 SINK
142 QSF
143 NRST
144 SCLK

FDC37C665


FDC37C665
1 DENSEL
2 MTR0
3 DS1
4 DS0
5 MTR1
6 VSS
7 DIR
8 STEP
9 WDATA
10 WGATE
11 HDSEL
12 INDEX
13 TRK0
14 WRTPRT
15 VCC
16 RDATA
17 DSKCHG
18 DRATE1/MEDIA_ID1
19 DRATE0/MEDIA_ID0
20 X1/CLK1
21 X2/CLK2
22 IDED7
23 IDEENLO
24 IDEENHI
25 HDCS0
26 HDCS1
27 IOCS16
28 A0
29 A1
30 A2
31 A3
32 A4
33 A5
34 A6
35 TC
36 DACK
37 IRQ3
38 IRQ4
39 PINTR
40 FINTR
41 A7
42 A8
43 A9
44 IOR
45 IOW
46 AEN
47 VSS
48 D0
49 D1
50 D2
51 D3
52 FDRQ
53 D4
54 D5
55 D6
56 D7
57 RESET
58 PWRGD
59 SLCT
60 PE
61 BUSY
62 ACK
63 PD7
64 PD6
65 PD5
66 PD4
67 VSS
68 PD3
69 PD2
70 PD1
71 PD0
72 VCC
73 SLCTIN
74 INIT
75 ERROR
76 AUTOFD
77 STROBE
78 RXD1
79 TXD1
80 DSR1
81 RTS1
82 CTS1
83 DTR1
84 RI1
85 DCD1
86 R12
87 DCD2
88 RXD2
89 TXD2
90 DSR2
91 RTS2
92 CTS2
93 DTR2
94 DRV2/ADRx
95 VSS
96 MTR2/PDACK
97 DS3/A10
98 DS2/PDIR
99 MTR3/PDRQ
100 IOCHRDY

IOMD


IOMD
1 NFIQ
2 NIRQ
3 RCLK
4 VSS
5 NMREQ
6 NPREQ
7 A[0]
8 A[1]
9 A[2]
10 A[3]
11 A[4]
12 A[5]
13 A[6]
14 A[7]
15 A[8]
16 A[9]
17 VSS
18 VDD
19 A[10]
20 A[11]
21 A[12]
22 A[13]
23 A[14]
24 A[15]
25 A[16]
26 A[17]
27 A[18]
28 A[19]
29 A[20]
30 A[21]
31 A[22]
32 A[23]
33 A[24]
34 A[25]
35 VDD
36 VSS
37 A[26]
38 A[27]
39 A[28]
40 NRW
41 NBW
42 IICD
43 IICC
44 TDI
45 TMS
46 TCK
47 TDO
48 NWBE
49 NRBE
50 NBLW
51 NBLR
52 CLK2
53 NPBOE
54 LMW
55 VSS
56 BD[0]
57 BD[1]
58 BD[2]
59 BD[3]
60 BD[4]
61 BD[5]
62 BD[6]
63 BD[7]
64 BD[8]
65 BD[9]
66 BD[10]
67 BD[11]
68 CLK16
69 VSS
70 VDD
71 REF8M
72 BD[12]
73 BD[13]
74 BD[14]
75 BD[15]
76 NEASIS
77 NIORQ
78 NIOGT
79 NBL
80 NINDEX
81 DREQ[0]
82 DREQ[1]
83 DREQ[2]
84 DREQ[3]
85 NIOR
86 NIOW
87 VDD
88 VSS
89 CLK64
90 POR
91 NRESET
92 NMS
93 READY
94 ID
95 NDACK[0]
96 NDACK[1]
97 NDACL[2]
98 NDACK[3]
99 VSS
100 NSIO
101 NDT[0]
102 NDT[1]
103 NSE
104 DSF
105 NVRAS
106 SC
107 PCLK
108 VSS
109 QSF
110 FLYBK
111 VNC
112 NSNDRQ
113 NSNDAK
114 NVIDRQ
115 NVIDAK
116 NCDOE
117 NPROG
118 RA[0]
119 RA[1]
120 RA[2]
121 VSS
122 VDD
123 RA[3]
124 RA[4]
125 RA[5]
126 RA[6]
127 RA[7]
128 RA[8]
129 RA[9]
130 VSS
131 RA[10]
132 RA[11]
133 NRAS[3]
134 NRAS[2]
135 NWE[1]
136 NRAS[1]
137 NRAS[0]
138 NWE[0]
139 VDD
140 VSS
141 NCAS[0]
142 NCAS[1]
143 NCAS[2]
144 NCAS[3]
145 SPDRQ
146 SCDRQ
147 MSY[1]
148 MSY[0]
149 MSX[1]
150 MSX[0]
151 NPIRQ
152 NPFIQ
153 NSPDACK
154 NSCDACK
155 NSNDCS
156 NCCS
157 NSCCS
158 TC
159 NCDACK
160 VSS
161 KDATA
162 KCLK
163 NSCIRQ
164 NSINTR
165 NFINTR
166 PINTR
167 FDRQ
168 NIEXT
169 D[0]
170 D[1]
171 D[2]
172 D[3]
173 VSS
174 VDD
175 D[4]
176 D[5]
177 D[6]
178 D[7]
179 D[8]
180 D[9]
181 D[10]
182 D[11]
183 D[12]
184 D[13]
185 D[14]
186 D[15]
187 D[16]
188 D[17]
189 D[18]
190 D[19]
191 VDD
192 VSS
193 D[20]
194 D[21]
195 D[22]
196 D[23]
197 D[24]
198 D[25]
199 D[26]
200 D[27]
201 D[28]
202 D[29]
203 D[30]
204 D[31]
205 NROMCS
206 VSS
207 MCLK
208 DBE

Appendix E – Mechanical and electrical data

Power supply unit

70 Watt PSU Continuous power supply:	69 Watts
Total surge output power:	95 Watts (< 10 seconds)
103 Watt PSU Continuous power supply:	103 Watts
Total surge output power:	139 Watts (< 10 seconds)

Mains input

AC Mains power is applied via an IEC 320 style male inlet on the Risc PC rear panel.

Line input voltage range:	198 - 254.4 Volts ac, single phase at 47 - 63 Hertz.
	98 - 132 Volts ac, single phase at 47 - 63 Hertz (PSU link selectable).

Mains output (switched)

IEC 320 style female outlet socket. Mounted on rear panel of power supply.

Low voltage output leadsets and sockets

Two 5.25 inch drive bays are catered for by two 4 way floating lead sets terminated in 4 way sockets and one floppy drive is catered for by one 4 way lead set. Pinouts of these connectors are given in the relevant area of the text in Section 2 of this manual, however, the voltage/colour scheme is the same for all connectors and is given below. The fourth output leadset is for the main PCB and its pinout is as follows:

Table 5.1: Main PCB power supply socket

Pin	Colour	Connection
1	Red	+5V (Vo1)
2	Black	0V
3	Yellow	+12V (Vo2)
4	Red	+5V (Vo1)
5	Black	0V
6	Blue	-12V (Vo3)

Output voltages and currents

	Output Voltage Vo1	Output Voltage Vo2	Output Voltage Vo3	Units
Nominal Voltage	+5.1	+12.0	-12.0	Volts DC
Tolerance	+2%,-4%	+/-7%	+/-7%	
Min O/P Current (Imin)	0.50	0.10	0.00	Amps DC
Max Continuous O/P Current 70W (Imax)	7.90	2.05	0.25	Amps DC
Max Continuous O/P Current 103W (Imax)	11.00	3.60	0.25	Amps DC
Output Currents, surge 70W	9.40	3.55	0.35	Amps DC
Output Currents, surge 103W	12.50	6.10	0.35	Amps DC
Output Currents, surge duration	4.0	10	-	Seconds
Ripple & Noise, pk-pk	50	100	50	mV

System power budget

The following table defines the maximum current drain permissible on each of the following interfaces:

Mouse interface	+5V	80mA
Keyboard interface	+5V	300 mA
Monitor interface	+5V	250 mA
Expansion cards (per card)	+5V +12V -5V	1 A 250 mA 10 mA

Mechanical data

The Risc PC case is moulded from Bayer Bayblend FR90 – a high-impact-resistant plastic made from a mixture of ABS and polycarbonate. The plastic colour is specified as: 'Pantone Cool Grey 2'. On some models the inside of the case may be sprayed with nickel loaded paint in order to cut down electrical emissions.

The modular sandwich-like construction consists (in a minimum configuration) of a top, centre-section and base (which holds the PCB). The top is held on with two glass-reinforced nylon twist-lock pins, and the centre-section by two more. The centre section can be lifted out by unplugging the drives and lifting it out, revealing the PCB and power supply.

The floppy and hard disc drives are held in place with spring clips, although some early production machines have screw fasteners for the floppy as well. The PCB clips into place and is additionally held with one screw which provides good earth contact with the case. The PSU is held in place with one screw.

The centre-section can hold one 3.5in drive, one 5.25in drive and up to two expansion cards. By adding subsequent middle sections (along with suitably longer twist-lock pins) a system may be built up in units of the above each time.

Note: The PSU may need to be upgraded if more than two sections are used.

Case Dimensions

Height (standard): 117mm

Height (two centre-sections): 182mm

Height of each extra centre: 65mm

Width: 355mm

Depth: 383.4mm

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Do you like the way the information is presented?

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